# 5A 2-4 Cell Buck-Boost Switching Battery Charger

## General Description

The RT9492 is a highly-integrated 5A Buck-Boost switch mode battery charge management and system power path management device for 2-4 cell Li-Ion and Li-polymer battery. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. The $I^2C$ serial interface with charging and system settings makes the device a truly flexible solution.

The recommended junction temperature range is –40°C to 130°C, and the ambient temperature range is –40°C to 85°C.

## Ordering Information

RT9492 □□□

- Pin 1 Orientation
  (2): Quadrant 2, Follow EIA-481
- Package Type(1)
  QVF: VQFN-29TL 4x4 (FC) (V-Type)
- Lead Plating System(2)
  G: Richtek Green Policy Compliant

**Note 1**.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

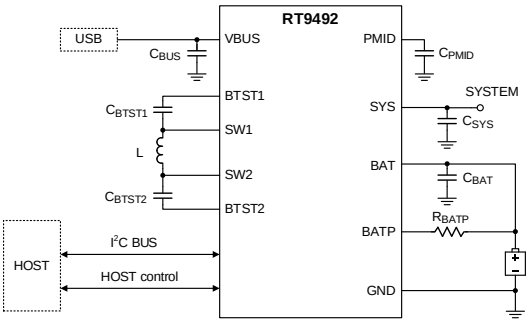
## Applications

- Smart Phone/Tablet/Chrome Book
- Drone
- Portable Device and Accessory

## Features

- **High Efficiency, 750kHz/1MHz/1.5MHz Programmable Frequencies, Synchronous Switch-Mode Buck-Boost Charger**
  - **96.7% Charge Efficiency at 2A with 9V Input and 8V Battery**
  - **Support 3.6V to 24V Input Voltage Range**
  - **Average Input Current Regulation (AICR)**
  - **Minimum Input Voltage Regulation (MIVR)**
- **Support USB On-The-Go (OTG)**
  - **93.4% OTG Efficiency at 2A with 8.4V Battery and 5V Output**
  - **Output Voltage with 10mV Resolution to Support USB-PD**
  - **BAT Current Limit Regulation (BCLR)**
- **Support Dual Input Selection**
- **Support BC1.2, Host Mode and FRS/Seamless**
- **Low Battery Quiescent Current**
- **High Accuracy for Charger CV and ICHG**
- **Protection**
  - **Over-Temperature Protection (OTP)**
  - **Junction Thermal Regulation (JTR)**
  - **Input Protection (VAC OVP/VBUS OVP/OCP)**
  - **Battery Overvoltage Protection (VBAT OVP)**
  - **System Voltage Protection (VSYS OVP/UVP)**
  - **System Over-Load Protection (VSYS OLP)**
  - **Cycle-by-Cycle Overcurrent Protection (OCP)**
  - **OTG Low Battery Protection (OTG LBP)**
  - **OTG Voltage Protection (OTG OVP/UVP)**

## Simplified Application Circuit

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## Marking Information

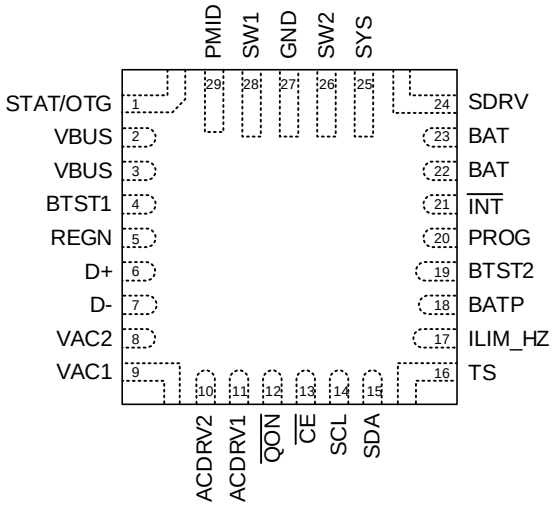
GT=: Product Code
YMDNN: Date Code

## Device Comparison

| Part Number | RT9490 | RT9492 |
|---|---|---|
| DEVICE_ID, REG0x48[6:3] | 1100 | 1110 |
| VAC_OVP, REG0x10[5:4] | 7V (Default), 12V, 22V, 26V | 7V, 12V, 18V, 26V (Default) |
| $\overline{PG}$ Pin | Yes | NA |
| IBAT Pin | Yes | NA |
| BATN Pin | Yes | NA |
| TS_ADC LSB, REG0x3F[15:0] | 0.098% | 0.0963% |
| Package | WL-CSP-56B 2.93x3.46 (BSC) | VQFN-29TL 4x4 (FC) |

## Pin Configuration

(TOP VIEW)




VQFN-29TL 4x4 (FC)

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## Functional Pin Description

| Pin No. | Pin Name | I/O | Pin Function |
|---|---|---|---|
| 1 | STAT/OTG | DIO | Open-drain charger status output. Connect the STAT pin to a logic rail via 2.2kΩ to 10kΩ resistor. The STAT pin indicates charger status.<br>Open-drain OTG mode enable control input. Active high. Connect the OTG pin to a logic rail via 2.2kΩ to 10kΩ resistor. |
| 2, 3 | VBUS | P | Charger input voltage. The internal current sensing circuit is connected between VBUS and PMID. Connect two 10μF capacitors from VBUS to GND and place as close as possible to VBUS. |
| 4 | BTST1 | P | The high-side switching MOSFET (Q1) driver positive supply. Internally, the BTST1 is connected to the cathode of the bootstrap diode. Connect the 47nF bootstrap capacitor from BTST1 to SW1. |
| 5 | REGN | P | PWM low-side driver and internal supply output. Internally, REGN is connected to the anode of the bootstrap diode. Connect a 4.7μF capacitor from REGN to GND. The capacitor should be placed close to the IC. REGN must be used only for RT9492 relative functions. |
| 6 | D+ | AIO | Positive line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary, secondary detection in BC1.2 and manual control mode. |
| 7 | D- | AIO | Negative line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary, secondary detection in BC1.2 and manual control mode. |
| 8 | VAC2 | AI | VAC2 voltage sensing. When a voltage on VAC2 is above VAC2_UVLO, it represents input source plug in on port2. When there is no external AC-RBFET2, the VAC2 must connect to VBUS |
| 9 | VAC1 | AI | VAC1 voltage sensing. When a voltage on VAC1 is above VAC1_UVLO, it represents input source plug in on port1. When there is no external AC-RBFET1, the VAC1 must connect to VBUS |
| 10 | ACDRV2 | P | External AC-RB N-channel FET gate driver output. The ACDRV2 is connected to external AC-RBFET2, the charger turns on AC-RBFET2 by increasing ACDRV2 voltage 5V above the AC-RBFET2 drain when the turn on condition is valid. When there is no external AC-RBFET2, the ACDRV2 must connect to GND. |
| 11 | ACDRV1 | P | External AC-RB N-channel FET gate driver output. The ACDRV1 is connected to external AC-RBFET1, the charger turns on AC-RBFET1 by increasing ACDRV1 voltage 5V above the AC-RBFET1 drain when the turn on condition is valid. When there is no external AC-RBFET1, the ACDRV1 must connect to GND. |
| 12 | $\overline{\text{QON}}$ | DI | Ship FET control input. When the device is in ship mode, a logic low duration with $t_{QON_EXIT_SHIP_DLY}$ turns on Ship FET to exit ship mode. A logic low duration with $t_{QON_RST}$ turns off the ship FET and stop converter switching for $t_{SYS_RST}$ and resume to provide system reset. Pull-High to internal bias circuit via 200kΩ resistor. |
| 13 | $\overline{\text{CE}}$ | DI | Charge enable pin. Active low. When this pin is driven low and REG_CHG_EN = 1, battery charging is enabled. Do NOT leave this pin floating. |
| 14 | SCL | DI | $I^2C$ interface clock. Connect SCL to the logic rail through a 10kΩ resistor. |
| 15 | SDA | DIO | $I^2C$ interface clock. Connect SDA to the logic rail through a 10kΩ resistor. |

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| Pin No. | Pin Name | I/O | Pin Function |
|---|---|---|---|
| 16 | TS | AI | Temperature qualification voltage input to support JEITA profile. Connect a negative temperature coefficient thermistor (103AT). Program temperature window with a resistor divider from REGN to TS to GND. The resistors used for resistor divider recommend 1% resistance tolerance. Charge suspends when TS pin voltage is out of range. When TS pin is not used, connect a 10kΩ resistor from REGN to TS and a 10kΩ resistor from TS to GND. |
| 17 | ILIM_HZ | AI | Input current limit setting and HZ mode control. A resistor divider is connected to ILIM_HZ pin by pull up resistors from REGN to GND. The pin voltage is calculated as $V_{ILIM_HZ}$ = 1V + 800mΩ x ILIM, where ILIM is target input current limit. The input current limit for charger is the lower setting between ILIM_HZ and AICR register. When the pin voltage is below 0.75V, the buck-boost converter stops switching and REGN on. When the pin voltage is higher than 1V, the converter resumes switching. |
| 18 | BATP | AI | Positive battery voltage sensing. Connect to the positive terminal of battery pack. It is recommended to place 100Ω series resistor between BATP and the positive terminal of battery pack. |
| 19 | BTST2 | P | The high-side switching MOSFET (Q4) driver positive supply. Internally, the BTST2 is connected to the cathode of the bootstrap diode. Connect the 47nF bootstrap capacitor from BTST2 to SW2. |
| 20 | PROG | AI | Charger POR default setting program. A resistor is connected from PROG to GND to set battery cells for default charging profile and switching frequency. The resistor connected to PROG is recommended to be 1% or 2% resistance tolerance. |
| 21 | $\overline{INT}$ | DO | Open-drain interrupt output. Active low. Connect the $\overline{INT}$ to a logic rail through 10kΩ resistor. The $\overline{INT}$ pin sends active low pulse to host to report charger device status and fault. |
| 22, 23 | BAT | P | Battery connection point to the positive terminal of the battery pack. The internal current sensing circuit is connected between SYS and BAT. Connect two 10μF capacitors from BAT to GND and place as close as possible to BAT. |
| 24 | SDRV | P | External Ship N-channel FET gate driver output. The SDRV is connected to external ship FET, the SDRV is always turned off when in ship or shutdown mode. Without using ship FET, must connect a 1nF/50V capacitor from SDRV to GND. |
| 25 | SYS | P | Charger output connection point. Connected to the drain of high-side switching MOSFET (Q4) and the internal current sensing circuit between SYS and BAT. Connect five 10μF and a 0.1μF capacitors from SYS to GND and place as close as possible to SYS. |
| 26 | SW2 | P | Switching node two connecting to output inductor. Internally SW2 is connected to the drain of the low-side switching MOSFET (Q3) and the source of the high-side switching MOSFET (Q4). |
| 27 | GND | P | Power Ground |
| 28 | SW1 | P | Switching node one connecting to output inductor. Internally SW1 is connected to the source of the high-side switching MOSFET (Q1) and the drain of the low-side switching MOSFET (Q2). |
| 29 | PMID | P | Connected to the drain of high-side switching MOSFET (Q1). Connect three 10μF and a 0.1μF capacitors from PMID to GND and place as close as possible to PMID. |

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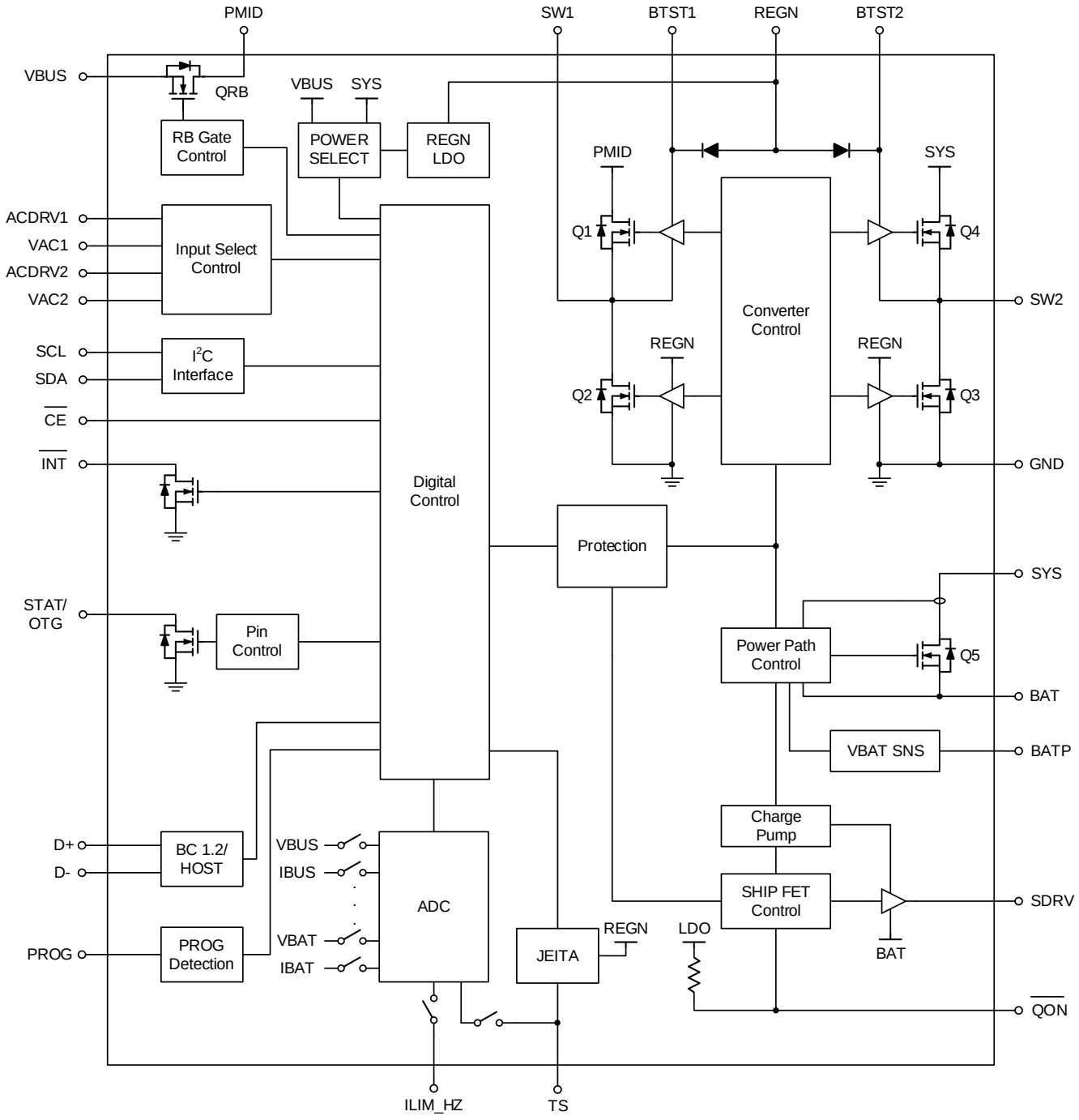
## Functional Block Diagram

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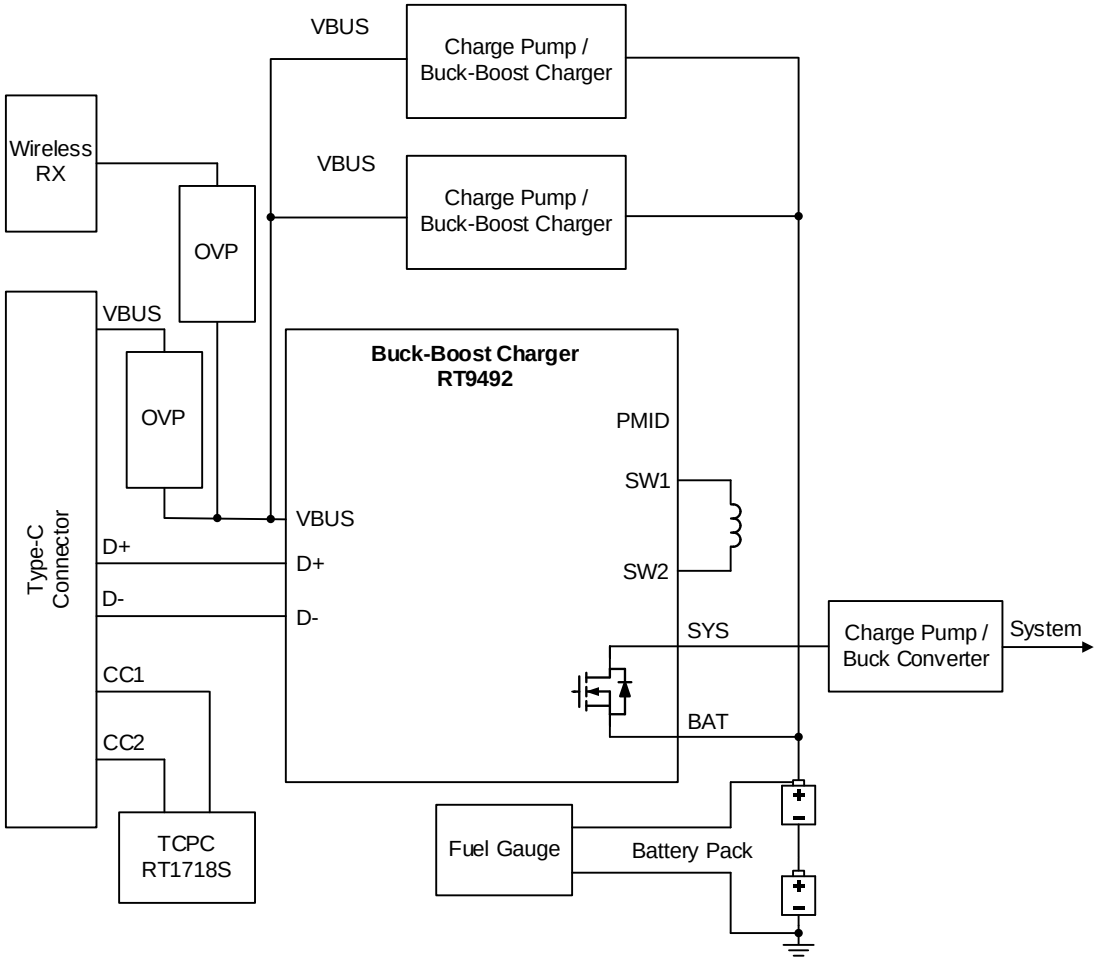
## System Block Diagram

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## Absolute Maximum Ratings (Note 2)

- Voltage Sense Pin Voltage, VAC1, VAC2 ---------- –2V to 30V
- Supply Pin Voltage, VBUS ---------- –2V to 30V
- Terminal Pin Voltage, PMID ---------- –0.3V to 30V
- Terminal Pin Voltage, ACDRV1, ACDRV2, BTST1 ---------- –0.3V to 32V
- Terminal Pin Voltage, BTST2 ---------- –0.3V to 29V
- Terminal Pin Voltage, SW1 ---------- –2V (50ns) to 30V
- Terminal Pin Voltage, SW2 ---------- –2V (50ns) to 23V
- Terminal Pin Voltage, SYS ---------- –0.3V to 23V
- Supply Pin Voltage, BAT ---------- –0.3V to 20V
- Voltage Sense Pin Voltage, BATP ---------- –0.3V to 20V
- Terminal Pin Voltage, SDRV ---------- –0.3V to 26V
- Terminal Pin Voltage, PMID-VBUS ---------- –0.3V to 6V
- Terminal Pin Voltage, BTST1-SW1, BTST2-SW2 ---------- –0.3V to 6V
- Terminal Pin Voltage, SYS-BAT ---------- –0.3V to 16V
- Terminal Pin Voltage, SDRV-BAT ---------- –0.3V to 6V
- Other Pins Voltage, STAT/OTG, SCL, SDA, $\overline{INT}$, $\overline{CE}$, D+, D- ---------- –0.3V to 6V
- Other Pins Voltage for REGN, TS, $\overline{QON}$, ILIM_HZ, PROG ---------- –0.3V to 6V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  VQFN-29TL 4x4 (FC) ---------- 2.38W
- Package Thermal Resistance (Note 3)
  VQFN-29TL 4x4 (FC), $\theta_{JA}$ ---------- 44°C/W
  VQFN-29TL 4x4 (FC), $\theta_{JC}$ ---------- 3.6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –55°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) ---------- 2kV

## Recommended Operating Conditions (Note 5)

- Voltage Sense Pin Voltage, VAC1, VAC2 ---------- 3.6V to 24V
- Supply Input Voltage Range, VBUS ---------- 3.6V to 24V
- Maximum Input Current, IBUS ---------- 3.3A
- Maximum Input Current, IOTG ---------- 3.32A
- Maximum Output Current (SW2), ISYS (Note 6) ---------- 5A
- Maximum Battery Voltage, VBAT ---------- 18.8V
- Maximum Charge Current, IBAT ---------- 5A
- Maximum Discharge Current, IBAT ---------- 10A
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 130°C

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## Electrical Characteristics

($V_{BUS_UVLO}$ < $V_{BUS}$ < $V_{BUS_OVP}$, $T_J$ = 25°C, unless otherwise specified) (Note 7)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Quiescent Current** | | | | | | |
| Battery Discharge Current (BATP) in Ship Mode | $I_{Q_BAT_OFF}$ | BATP = 8V, No VBUS, $I^2C$ enabled, SYS no load, in ship mode, measure IBAT | -- | 2.5 | 6 | μA |
| Battery Discharge Current (BATP) in Shutdown Mode | $I_{SD_BAT_OFF}$ | BATP = 8V, No VBUS, $I^2C$ disable, SYS no load, in shutdown mode, measure IBAT | -- | 0.6 | 0.9 | μA |
| Battery Discharge Current (BATP, BAT) in the Battery Only Mode, Q5 is Enabled | $I_{Q_BAT_ON}$ | $V_{BAT}$ = 8V, No VBUS, Q5 is enabled, $I^2C$ enabled, SYS no load, measure IBAT | -- | 18 | 23 | μA |
| Battery Discharge Current (BATP, BAT) in the Battery Only Mode, Q5 is Enabled | $I_{Q_BAT_ADC_ON}$ | $V_{BAT}$ = 8V, No VBUS, Q5 is enabled, $I^2C$ enabled, ADC VBAT enabled, SYS no load, measure IBAT | -- | 650 | -- | μA |
| Input Supply Current (VAC) in HZ mode | $I_{VAC_HZ}$ | $V_{AC}$ = 5V, HZ mode, no battery, ACDRV enable | -- | 500 | 550 | μA |
| Input Supply Current (VBUS) in HZ mode | $I_{VBUS_HZ}$ | $V_{BUS}$ = 5V, HZ mode, no battery, ACDRV disable | -- | 354 | 440 | μA |
| Input Supply Current (VBUS) | $I_{BUS_SW}$ | $V_{BUS}$ = 15V, VBAT = 8V, charge disabled, converter switching, ISYS = 0A, OOA disabled | -- | 3 | -- | mA |
| | | $V_{BUS}$ = 15V, VBAT = 8V, charge disabled, converter switching, ISYS = 0A, OOA enable | -- | 5 | -- | |
| Battery Discharge Current (BATP, BAT) in OTG Mode | $I_{BAT_OTG}$ | $V_{BAT}$ = 8V, VOTG = 5V, OTG mode enabled, converter switching, IBUS = 0A, OOA disabled | -- | 2 | -- | mA |
| | | $V_{BAT}$ = 8V, VOTG = 5V, OTG mode enabled, converter switching, IBUS = 0A, OOA enabled | -- | 5 | -- | |
| **VAC, VBUS and BAT Power** | | | | | | |
| VAC rising threshold to Turn On the ACDRV | $V_{VAC_RISE}$ | $V_{AC}$ rising until ACFET turn on, measure VAC, VBUS, ACDRV1 and ACDRV2 | -- | 3.4 | 3.5 | V |
| VAC falling threshold to Turn Off the ACDRV | $V_{VAC_FALL}$ | $V_{AC}$ falling until ACFET turn off, measure VAC, VBUS, ACDRV1 and ACDRV2 | 3 | 3.2 | -- | V |
| VBUS Rising for Active $I^2C$, No Battery | $V_{BUS_UVLO}$ | VBUS only, $V_{BUS}$ rising to active $I^2C$ | 3.45 | 3.6 | 3.75 | V |
| VBUS Falling to Turn Off $I^2C$, No Battery | | VBUS only, $V_{BUS}$ falling to turn off $I^2C$ | -- | 2.4 | 2.6 | V |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VBUS Rising Threshold to Start Switching | $V_{VBUS_RISE}$ | VBUS rising | 3.45 | 3.6 | 3.75 | V |
| VBUS Falling Threshold to Turn off REGN | $V_{BUS_FALL}$ | $V_{BUS}$ falling | 3.03 | 3.2 | 3.3 | V |
| VAC 26V Overvoltage Rising Threshold | $V_{AC_OVP}$ | $V_{AC}$ rising, VAC_OVP[1:0] = 00, for both VAC1 and VAC2 | 25.2 | 26 | 26.8 | V |
| VAC 26V Overvoltage Falling Threshold | | $V_{AC}$ falling, VAC_OVP[1:0] = 00, for both VAC1 and VAC2 | 24.4 | 25.2 | 26 | |
| VAC 18V Overvoltage rising threshold | | $V_{AC}$ rising, VAC_OVP[1:0] = 01, for both VAC1 and VAC2 | 17.4 | 18 | 18.6 | |
| VAC 18V Overvoltage falling threshold | | $V_{AC}$ falling, VAC_OVP[1:0] = 01, for both VAC1 and VAC2 | 16.9 | 17.5 | 18.1 | |
| VAC 12V Overvoltage Rising Threshold | | $V_{AC}$ rising, VAC_OVP[1:0] = 10, for both VAC1 and VAC2 | 11.6 | 12 | 12.4 | |
| VAC 12V Overvoltage Falling Threshold | | $V_{AC}$ falling, VAC_OVP[1:0] = 10, for both VAC1 and VAC2 | 11.2 | 11.6 | 12 | |
| VAC 7V Overvoltage Rising Threshold | | $V_{AC}$ rising, VAC_OVP[1:0] = 11, for both VAC1 and VAC2 | 6.6 | 7 | 7.4 | |
| VAC 7V Overvoltage Falling Threshold | | $V_{AC}$ falling, VAC_OVP[1:0] = 11, for both VAC1 and VAC2 | 6.5 | 6.8 | 7.1 | |
| VBUS Overvoltage Rising Threshold | $V_{BUS_OVP}$ | $V_{BUS}$ rising | 24 | 25 | 26.2 | V |
| VBUS Overvoltage Falling Threshold | | $V_{BUS}$ falling | 23 | 24 | 24.8 | |
| IBUS Overcurrent Rising Threshold | $I_{BUS_OCP}$ | $I_{BUS}$ rising | -- | 8 | -- | A |
| BAT for turn on Q5 and Active $I^2C$ | $V_{BAT_UVLO}$ | $V_{BAT}$ rising | 2.4 | 2.6 | 2.7 | V |
| BAT for turn off Q5 and $I^2C$ | | $V_{BAT}$ falling | 2.2 | 2.4 | 2.5 | |
| BATP for turn on Ship FET and Active $I^2C$ | $V_{BATP_UVLO}$ | $V_{BATP}$ rising | 3.3 | 3.4 | 3.5 | V |
| BATP for turn off $I^2C$ and Ship FET | | $V_{BATP}$ falling | 2.2 | 2.4 | 2.5 | |
| Bad Adapter Detection Falling Threshold | $V_{BUS_MIN}$ | $V_{BUS}$ falling | 3.3 | 3.4 | 3.5 | V |
| Bad Adapter Detection Hysteresis | $V_{BUS_MIN_HYS}$ | $V_{BUS}$ rising | 140 | 200 | 250 | mV |
| Bad Adapter Detection Sink Source | $R_{BADSRC}$ | Sink source from $V_{BUS}$ to GND, $V_{BUS}$ = 5V | -- | 1.1 | -- | kΩ |
| **Power Path** | | | | | | |
| SYS Minimum Regulation Voltage Setting Range | $V_{SYSMIN_RANGE}$ | $V_{SYSMIN}$ regulation range, measured on SYS | 2.5 | -- | 16 | V |
| SYS Minimum Regulation Voltage Step | $V_{SYSMIN_STEP}$ | | -- | 250 | -- | mV |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SYS Minimum Regulation Voltage | $V_{SYSMIN}$ | $V_{BAT}$ < $V_{SYSMIN}$, Q5 disabled/ enable | $V_{SYSMIN}$ | $V_{SYSMIN}$ + 0.2 | -- | V |
| SYS Minimum Regulation Voltage Accuracy | $V_{SYSMIN_ACC}$ | $V_{SYSMIN}$ = 7V | –2 | -- | 2 | % |
| SYS Regulation Voltage Range | $V_{SYSREG_RANGE}$ | | 3.3 | -- | 19.1 | V |
| SYS Regulation Voltage | $V_{SYSREG}$ | $V_{BAT}$ = 16.8V, $V_{BAT}$ > $V_{SYSMIN}$, Q5 disabled | 16.9 | 17.1 | 17.3 | V |
| | | $V_{BAT}$ =12.6V, $V_{BAT}$ > $V_{SYSMIN}$, Q5 disabled | 12.72 | 12.9 | 13.14 | |
| | | $V_{BAT}$ = 8.4V, $V_{BAT}$ > $V_{SYSMIN}$, Q5 disabled | 8.53 | 8.7 | 8.87 | |
| VSYS Overvoltage Rising Threshold | $V_{SYS_OVP}$ | As a percentage of the system regulation voltage, the converter stops switching when $V_{SYS}$ rises | 105.5 | 110 | 112.5 | % |
| VSYS Overvoltage Falling Threshold | | As a percentage of the system regulation voltage, the converter re-start switching when $V_{SYS}$ falling | 95.5 | 100 | 102.5 | |
| VSYS Overvoltage Sink Source | $R_{SYS_OVP}$ | Sink source from $V_{SYS}$ to GND | -- | 0.85 | -- | kΩ |
| VSYS Short Voltage Falling Threshold | $V_{SYS_SHORT}$ | VSYS falling | 2.1 | 2.2 | 2.3 | V |
| **Battery Charger** | | | | | | |
| Charge Voltage Setting Range | $V_{BAT_REG_RANGE}$ | | 5 | -- | 18.8 | V |
| Charge Voltage Step | $V_{BAT_REG_STEP}$ | | -- | 10 | -- | mV |
| Charge Voltage Setting Accuracy | $V_{BAT_REG_ACC}$ | $V_{BAT_REG}$ = 8.4V | –0.3 | -- | 0.3 | % |
| | | $V_{BAT_REG}$ = 12.6V | –0.3 | -- | 0.3 | |
| | | $V_{BAT_REG}$ = 16.8V | –0.5 | -- | 0.5 | |
| Charge Current Regulation Setting Range | $I_{CHG_REG_RANGE}$ | | 150 | -- | 5000 | mA |
| Charge Current Regulation Step | $I_{CHG_REG_STEP}$ | | -- | 10 | -- | mA |
| Charge Current Regulation Accuracy | $I_{CHG_REG_ACC}$ | $I_{CHG_REG}$ = 2A, $V_{SYSMIN}$ = 7V, $V_{BAT}$ = 8V (Note 7) | –3.5 | -- | 3.5 | % |
| | | $I_{CHG_REG}$ = 1A, $V_{SYSMIN}$ = 7V, $V_{BAT}$ = 8V | –4 | -- | 4 | |
| | | $I_{CHG_REG}$ = 0.5A, $V_{SYSMIN}$ = 7V, $V_{BAT}$ = 8V | –7.5 | -- | 7.5 | |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Pre-Charge Rising Threshold | $V_{PRE_CHG_RISE}$ | $V_{PRE_CHG}$ = 15% x $V_{BAT_REG}$, Pre-charge to Fast-charge, $V_{BAT_REG}$ = 18.8V | 13 | 15 | 17 | % |
| | | $V_{PRE_CHG}$ = 62% x $V_{BAT_REG}$, Pre-charge to Fast-charge, $V_{BAT_REG}$ = 8.4V | 60.5 | 62 | 63.5 | |
| | | $V_{PRE_CHG}$ = 66.5% x $V_{BAT_REG}$, Pre-charge to Fast-charge, $V_{BAT_REG}$ = 8.4V | 65 | 66.5 | 68 | |
| | | $V_{PRE_CHG}$ = 71.5% x $V_{BAT_REG}$, Pre-charge to Fast-charge, $V_{BAT_REG}$ = 8.4V | 70 | 71.5 | 73 | |
| Pre-Charge Hysteresis | $V_{PRE_CHG_HYS}$ | Fast-charge to Pre-charge | -- | 1.5 | -- | % |
| Pre-Charge Current Setting Range | $I_{PRE_CHG_RANGE}$ | Default = 120mA | 120 | -- | 2000 | mA |
| Pre-Charge Current Step | $I_{PRE_CHG_STEP}$ | | -- | 40 | -- | mA |
| Pre-Charge Accuracy | $I_{PRE_CHG_ACC}$ | $I_{PRE_CHG}$ = 200mA, $V_{SYS_MIN}$ = 7V, $V_{BAT}$ = 6.5V | –15 | -- | 15 | % |
| End-Of-Charge Current Setting Range | $I_{EOC_CHG_RANGE}$ | Default = 200mA | 120 | -- | 1000 | mA |
| End-Of-Charge Current Step | $I_{EOC_CHG_STEP}$ | | -- | 40 | -- | mA |
| End-Of-Charge Accuracy (Note 8) | $I_{EOC_CHG_ACC}$ | $I_{EOC_CHG}$ = 120mA, DIS_EOC_FCCM = 0 $V_{BUS}$ = 15V, $V_{BAT}$ = 8.4V | –20 | -- | 20 | % |
| | | $I_{EOC_CHG}$ = 200mA, DIS_EOC_FCCM = 0 $V_{BUS}$ = 15V, $V_{BAT}$ = 8.4V | –15 | -- | 15 | |
| | | $I_{EOC_CHG}$ = 480mA, DIS_EOC_FCCM = 0 $V_{BUS}$ = 15V, $V_{BAT}$ = 8.4V | –10 | -- | 10 | |
| Trickle-Charge Falling Threshold | $V_{TRICKLE_CHG_FALL}$ | $V_{BAT}$ falling | 1.8 | 2 | 2.2 | V |
| Trickle-Charge Rising Threshold | $V_{TRICKLE_CHG_RISE}$ | $V_{BAT}$ rising | 2.05 | 2.25 | 2.45 | V |
| Trickle-Charge Current | $I_{TRICKLE_CHG}$ | $V_{BAT}$ < $V_{TRICKLE_CHG_RISE}$ | 80 | 100 | 120 | mA |
| Re-Charge Threshold Below VBAT_REG | $V_{RE_CHG}$ | $V_{BAT}$ falling, $V_{RECHG}$ = 200mV, $V_{BUS}$ = 15V, $V_{BAT_REG}$ = 8.4V | 180 | 200 | 230 | mV |
| **Input Voltage and Current Regulation** | | | | | | |
| Minimum Input Voltage Regulation Setting Range | $V_{MIVR_RANGE}$ | | 3.6 | -- | 22 | V |
| Minimum Input Voltage Regulation Step | $V_{MIVR_STEP}$ | | -- | 100 | -- | mV |
| Minimum Input Voltage Regulation Accuracy | $V_{MIVR_ACC}$ | $V_{MIVR}$ = 10.6V | –1 | -- | 1 | % |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Average Input Current Regulation Setting Range | $I_{AICR_RANGE}$ | | 0.1 | -- | 3.3 | A |
| Average Input Current Regulation Step | $I_{AICR_STEP}$ | | -- | 10 | -- | mA |
| Average Input Current Regulation Accuracy | $I_{AICR_ACC}$ | $V_{BUS}$ = 15V, $I_{AICR}$ = 500mA | 450 | 470 | 500 | mA |
| | | $V_{BUS}$ = 15V, $I_{AICR}$ = 1000mA | 900 | 950 | 1000 | |
| | | $V_{BUS}$ = 15V, $I_{AICR}$ = 2000mA (Note 7) | 1800 | 1900 | 2000 | |
| | | $V_{BUS}$ = 15V, $I_{AICR}$ > 2000mA (Note 7) | –9 | -- | 0 | % |
| **BAT Overvoltage Protection** | | | | | | |
| Battery Overvoltage Rising | $V_{BAT_OVP}$ | $V_{BAT}$ rising, as percentage of $V_{BAT_REG}$ | 103 | 104 | 105 | % |
| Battery Overvoltage Falling | | $V_{BAT}$ falling, as percentage of $V_{BAT_REG}$ | 101 | 102 | 103 | % |
| Battery Overvoltage Sink Source | $R_{BAT_OVP}$ | Sink source from $V_{BAT}$ to GND | -- | 1.1 | -- | kΩ |
| **Thermal Regulation and Shutdown** | | | | | | |
| Junction Thermal Regulation Setting Range | $T_{J_THREG_RANGE}$ | Default = 120°C | 60 | -- | 120 | °C |
| Junction Thermal Regulation Step | $T_{J_THREG_STEP}$ | | -- | 20 | -- | °C |
| Junction Thermal Regulation Accuracy | $T_{J_THREG_ACC}$ | $T_{J_THREG}$ = 120°C | -- | 120 | -- | °C |
| | | $T_{J_THREG}$ = 100°C | -- | 100 | -- | |
| | | $T_{J_THREG}$ = 80°C | -- | 80 | -- | |
| | | $T_{J_THREG}$ = 60°C | -- | 60 | -- | |
| Thermal Shutdown Rising | $T_{OTP}$ | $T_{J_THREG}$ = 150°C, Temperature rising (Note 7) | 130 | 150 | 170 | °C |
| | | $T_{J_THREG}$ = 130°C, Temperature rising (Note 7) | 110 | 130 | 150 | |
| | | $T_{J_THREG}$ = 120°C, Temperature rising (Note 7) | 100 | 120 | 140 | |
| | | $T_{J_THREG}$ = 85°C, Temperature rising (Note 7) | 65 | 85 | 105 | |
| Thermal Shutdown Hysteresis | $T_{OTP_HYS}$ | Temperature falling | -- | 30 | -- | °C |
| **NTC Monitor (Charger Mode)** | | | | | | |
| Battery Temperature COLD Threshold (0°C) | $V_{VTS_COLD}$ | $V_{TS}$ rising, the ratio of $V_{REGN}$ | 72.3 | 73.5 | 74.7 | % |
| | | $V_{TS}$ falling, the ratio of $V_{REGN}$ | 70.8 | 72 | 73.2 | |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Battery Temperature COOL Rising Threshold | $V_{VTS_COOL_RISE}$ | $V_{VTS_COOL}$ = 5°C, $V_{TS}$ rising, the ratio of $V_{REGN}$ (Note 7) | 70.6 | 71.1 | 71.6 | % |
| | | $V_{VTS_COOL}$ = 10°C, $V_{TS}$ rising, the ratio of $V_{REGN}$ | 67.4 | 68.5 | 69.6 | |
| | | $V_{VTS_COOL}$ = 15°C, $V_{TS}$ rising, the ratio of $V_{REGN}$ (Note 7) | 65 | 65.5 | 66 | |
| | | $V_{VTS_COOL}$ = 20°C, $V_{TS}$ rising, the ratio of $V_{REGN}$ (Note 7) | 61.9 | 62.4 | 62.9 | |
| Battery Temperature COOL Falling Threshold | $V_{VTS_COOL_FALL}$ | $V_{VTS_COOL}$ = 5°C, $V_{TS}$ falling, the ratio of $V_{REGN}$ (Note 7) | 69.3 | 69.8 | 70.3 | % |
| | | $V_{VTS_COOL}$ = 10°C, $V_{TS}$ falling, the ratio of $V_{REGN}$ | 65.9 | 67 | 68.1 | |
| | | $V_{VTS_COOL}$ = 15°C, $V_{TS}$ falling, the ratio of $V_{REGN}$ (Note 7) | 63.7 | 64.2 | 64.7 | |
| | | $V_{VTS_COOL}$ = 20°C, $V_{TS}$ falling, the ratio of $V_{REGN}$ (Note 7) | 60.6 | 61.1 | 61.6 | |
| Battery Temperature WARM Falling Threshold | $V_{VTS_WARM_FALL}$ | $V_{VTS_WARM}$ = 40°C, $V_{TS}$ falling, the ratio of $V_{REGN}$ (Note 7) | 47.9 | 48.4 | 48.9 | % |
| | | $V_{VTS_WARM}$ = 45°C, $V_{TS}$ falling, the ratio of $V_{REGN}$ | 44.2 | 45 | 45.8 | |
| | | $V_{VTS_WARM}$ = 50°C, $V_{TS}$ falling, the ratio of $V_{REGN}$ (Note 7) | 40.7 | 41.2 | 41.7 | |
| | | $V_{VTS_WARM}$ = 55°C, $V_{TS}$ falling, the ratio of $V_{REGN}$ (Note 7) | 37.2 | 37.7 | 38.2 | |
| Battery Temperature WARM Rising Threshold | $V_{VTS_WARM_RISE}$ | $V_{VTS_WARM}$ = 40°C, $V_{TS}$ rising, the ratio of $V_{REGN}$ (Note 7) | 49.2 | 49.7 | 50.2 | % |
| | | $V_{VTS_WARM}$ = 45°C, $V_{TS}$ rising, the ratio of $V_{REGN}$ | 45.2 | 46 | 46.8 | |
| | | $V_{VTS_WARM}$ = 50°C, $V_{TS}$ rising, the ratio of $V_{REGN}$ (Note 7) | 42 | 42.5 | 43 | |
| | | $V_{VTS_WARM}$ = 55°C, $V_{TS}$ rising, the ratio of $V_{REGN}$ (Note 7) | 38.5 | 39 | 39.5 | |
| Battery Temperature HOT Threshold (60°C) | $V_{VTS_HOT}$ | $V_{TS}$ falling, the ratio of $V_{REGN}$ | 33.4 | 34 | 34.7 | % |
| | | $V_{TS}$ rising, the ratio of $V_{REGN}$ | 34.9 | 35.5 | 36.1 | |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **NTC Monitor (OTG Mode)** | | | | | | |
| Battery Temperature COLD Rising Threshold OTG mode | $V_{VTS_COLD_OTG_RISE}$ | $V_{VTS_COLD_OTG}$ = –20°C, $V_{TS}$ rising, the ratio of $V_{REGN}$ (Note 7) | 78.7 | 80 | 81.3 | % |
| | | $V_{VTS_COLD_OTG}$ = –10°C, $V_{TS}$ rising, the ratio of $V_{REGN}$ | 75.7 | 77 | 78.3 | |
| Battery Temperature COLD Falling Threshold OTG mode | $V_{VTS_COLD_OTG_FALL}$ | $V_{VTS_COLD_OTG}$ = –20°C, $V_{TS}$ falling, the ratio of $V_{REGN}$ (Note 7) | 78.2 | 78.7 | 79.2 | % |
| | | $V_{VTS_COLD_OTG}$ = –10°C, $V_{TS}$ falling, the ratio of $V_{REGN}$ | 74.8 | 76 | 77.2 | |
| Battery Temperature HOT Falling Threshold OTG mode | $V_{VTS_HOT_OTG_FALL}$ | $V_{VTS_HOT_OTG}$ = 55°C, $V_{TS}$ falling, the ratio of $V_{REGN}$ (Note 7) | 37.2 | 37.7 | 38.2 | % |
| | | $V_{VTS_HOT_OTG}$ = 60°C, $V_{TS}$ falling, the ratio of $V_{REGN}$ | 33.9 | 34.5 | 35.1 | |
| | | $V_{VTS_HOT_OTG}$ = 65°C, $V_{TS}$ falling, the ratio of $V_{REGN}$ (Note 7) | 32 | 32.5 | 33 | |
| Battery Temperature HOT Rising Threshold OTG Mode | $V_{VTS_HOT_OTG_RISE}$ | $V_{VTS_HOT_OTG}$ = 55°C, $V_{TS}$ rising, the ratio of $V_{REGN}$ (Note 7) | 38.8 | 39.3 | 39.8 | % |
| | | $V_{VTS_HOT_OTG}$ = 60°C, $V_{TS}$ rising, the ratio of $V_{REGN}$ | 34.9 | 35.5 | 36.2 | |
| | | $V_{VTS_HOT_OTG}$ = 65°C, $V_{TS}$ rising, the ratio of $V_{REGN}$ (Note 7) | 32 | 32.5 | 33 | |
| **Overcurrent Threshold** | | | | | | |
| Q1 Cycle-by-Cycle Overcurrent Threshold | $I_{OCP_Q1}$ | | 8.55 | 10.5 | 12.25 | A |
| Q2 Cycle-by-Cycle Overcurrent Threshold | $I_{OCP_Q2}$ | | 6.8 | 7.5 | 8.25 | A |
| Q3 Cycle-by-Cycle Overcurrent Threshold | $I_{OCP_Q3}$ | | 6.8 | 7.5 | 8.25 | A |
| Q4 Cycle-by-Cycle Overcurrent Threshold | $I_{OCP_Q4}$ | | 8.55 | 10.5 | 12.25 | A |
| System Over-Load Threshold | $I_{OCP_BATFET}$ | | 11 | -- | -- | A |
| **Internal Sense Resistance and MOSFET Rdson** | | | | | | |
| Reverse-Blocking MOSFET (QRB) Turn on Resistance between VBUS and PMID | $R_{ON_QRB}$ | | -- | 9 | -- | mΩ |
| High-Side Switching MOSFET (Q1) Turn on Resistance between PMID and SW1 | $R_{ON_Q1}$ | $V_{REGN}$ = 4.9V | -- | 25 | -- | mΩ |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Low-Side Switching MOSFET (Q2) Turn on Resistance between SW1 and PGND | $R_{ON_Q2}$ | $V_{REGN}$ = 4.9V | -- | 34 | -- | mΩ |
| Low-Side Switching MOSFET(Q3) Turn on Resistance between SW2 and PGND | $R_{ON_Q3}$ | $V_{REGN}$ = 4.9V | -- | 28 | -- | mΩ |
| High-Side Switching MOSFET(Q4) Turn on Resistance between SW2 and SYS | $R_{ON_Q4}$ | $V_{REGN}$ = 4.9V | -- | 17 | -- | mΩ |
| BATFET (Q5) Turn on Resistance between SYS and BAT | $R_{ON_Q5}$ | | -- | 11 | -- | mΩ |
| **USB On-The-Go (OTG)** | | | | | | |
| OTG Low Battery Protection | $V_{OTG_LBP}$ | $V_{BAT}$ falling | 2.3 | 2.5 | 2.6 | V |
| | | $V_{BAT}$ rising | 2.5 | 2.7 | 2.9 | |
| OTG Voltage Limit Regulation Setting Range | $V_{OTG_CV_RANGE}$ | Default = 5V | 2.8 | -- | 22 | V |
| OTG Voltage Limit Regulation Step | $V_{OTG_CV_STEP}$ | | -- | 10 | -- | mV |
| OTG Voltage Limit Regulation Accuracy | $V_{OTG_CV_ACC}$ | $I_{VBUS}$ = 0A, $V_{OTG_REG}$ = 5V | –1.5 | -- | 1.5 | % |
| OTG Current Limit Regulation Setting Range | $I_{OTG_CC_RANGE}$ | Default = 3A | 0.12 | -- | 3.32 | A |
| OTG Current Limit Regulation Step | $I_{OTG_CC_STEP}$ | | -- | 40 | -- | mA |
| OTG Current Limit Regulation Accuracy | $I_{OTG_CC}$ | $I_{OTG_CC}$ = 3A, $V_{BAT}$ = 8V, $V_{OTG_CV}$ = 5V (Note 7) | –3 | -- | 3 | % |
| | | $I_{OTG_CC}$ = 1A, $V_{BAT}$ = 8V, $V_{OTG_CV}$ = 5V | –3 | -- | 3 | |
| | | $I_{OTG_CC}$ = 0.48A, $V_{BAT}$ = 8V, $V_{OTG_CV}$ = 5V | –10 | -- | 10 | |
| Battery Current Regulation in OTG Mode | $I_{OTG_BAT}$ | $I_{BAT_REG}$ = 3A, $V_{BAT}$ = 8V, $V_{OTG_CV}$ = 5V (Note 7) | 2.8 | 3 | 3.2 | A |
| | | $I_{BAT_REG}$ = 4A, $V_{BAT}$ = 8V, $V_{OTG_CV}$ = 5V (Note 7) | 3.8 | 4 | 4.2 | |
| | | $I_{BAT_REG}$ = 5A, $V_{BAT}$ = 8V, $V_{OTG_CV}$ = 5V (Note 7) | 4.8 | 5 | 5.2 | |
| OTG Overvoltage Threshold | $V_{OTG_OVP}$ | As percentage of $V_{OTG_CV}$, OTG mode, OOA disabled, $V_{BUS}$ rising | 104 | 113 | 120 | % |
| | | As percentage of $V_{OTG_CV}$, OTG mode, OOA disabled, $V_{BUS}$ falling | 90 | 98 | 104 | |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OTG Undervoltage Falling Threshold | $V_{OTG_UVP}$ | $V_{BUS}$ falling | 2.1 | 2.2 | 2.3 | V |
| **PWM** | | | | | | |
| PWM Switching Frequency | $f_{SW}$ | Oscillator frequency, $f_{SW}$ = 1.5MHz | -- | 1.5 | -- | MHz |
| | | Oscillator frequency, $f_{SW}$ = 750kHz | -- | 750 | -- | kHz |
| **REGN** | | | | | | |
| REGN LDO Output Voltage | $V_{REGN}$ | $V_{BUS}$ = 5V, $V_{BAT}$ = 8V, $I_{REGN}$ = 20mA, charge disabled, $I_{SYS}$ = 0A | 4.5 | 4.9 | 5.1 | V |
| | | $V_{BUS}$ = 15V, $V_{BAT}$ = 8V, $I_{REGN}$ = 20mA, charge disabled, $I_{SYS}$ = 0A | 4.5 | 4.9 | 5.2 | |
| REGN LDO Current Limit | $I_{REGN}$ | $V_{BUS}$ = 5V, $V_{BAT}$ = 8V, $V_{REGN}$ = 4.5V | 30 | -- | -- | mA |
| **Current Sink** | | | | | | |
| VAC1 Discharge Resistance | $R_{VAC1_DISCHG}$ | $V_{AC1_PD_EN}$ = 1, $V_{AC1}$ = 5V | -- | 1.1 | -- | kΩ |
| VAC2 Discharge Resistance | $R_{VAC2_DISCHG}$ | $V_{AC2_PD_EN}$ = 1, $V_{AC2}$ = 5V | -- | 1.1 | -- | kΩ |
| VBUS Discharge Resistance | $R_{VBUS_DISCHG}$ | $V_{BUS_PD_EN}$ = 1, $V_{BUS}$ = 5V | -- | 1.1 | -- | kΩ |
| **$I^2C$ Interface (SCL and SDA)** | | | | | | |
| Input SDA High Threshold Voltage | $V_{IH_SDA}$ | Pull high to 1.8V/1.2V | 0.84 | -- | -- | V |
| Input SDA Low Threshold Voltage | $V_{IL_SDA}$ | Pull high to 1.8V/1.2V | -- | -- | 0.4 | V |
| Output SDA Low Threshold Voltage | $V_{OL_SDA}$ | Sink current = 5mA | -- | -- | 0.4 | V |
| High Level SDA Leakage Current | $I_{BIAS_SDA}$ | Pull high to 1.8V | -- | -- | 1 | μA |
| Input SCL High Threshold Voltage | $V_{IH_SCL}$ | Pull high to 1.8V/1.2V | 0.84 | -- | -- | V |
| Input SCL Low Threshold Voltage | $V_{IL_SCL}$ | Pull high to 1.8V/1.2V | -- | -- | 0.4 | V |
| High Level SCL Leakage Current | $I_{BIAS_SCL}$ | Pull high to 1.8V | -- | -- | 1 | μA |
| SCL Clock Frequency | $f_{SCL}$ | | -- | -- | 3400 | kHz |
| **Control I/O Pin ($\overline{CE}$, $\overline{QON}$, and ILIM_HZ)** | | | | | | |
| Input $\overline{CE}$ High Threshold Voltage | $V_{IH_CE}$ | | 1.3 | -- | -- | V |
| Input $\overline{CE}$ LOW Threshold Voltage | $V_{IL_CE}$ | | -- | -- | 0.4 | V |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| High Level $\overline{CE}$ Leakage Current | $I_{BIAS_CE}$ | Pull high to 1.8V | -- | -- | 1 | μA |
| Input $\overline{QON}$ High Threshold Voltage | $V_{IH_QON}$ | | 1.3 | -- | -- | V |
| Input $\overline{QON}$ LOW Threshold Voltage | $V_{IL_QON}$ | | -- | -- | 0.4 | V |
| Internal $\overline{QON}$ Pull Up Voltage | $V_{QON}$ | | 2.8 | 3.1 | 3.4 | V |
| Internal $\overline{QON}$ Pull Up Resistance | $R_{QON}$ | | 185 | 200 | 230 | kΩ |
| Input ILIM_HZ High Threshold Voltage | $V_{IH_ILIM_HZ}$ | | 1 | -- | -- | V |
| Input ILIM_HZ Low Threshold Voltage | $V_{IL_ILIM_HZ}$ | | -- | -- | 0.75 | V |
| High Level LIMI_HZ Leakage Current | $I_{BIAS_ILIM_HZ}$ | $V_{ILIM_HIZ}$ = 4V | –1.5 | -- | 1.5 | μA |
| **Control I/O Pin ($\overline{INT}$ and STAT/OTG)** | | | | | | |
| Output $\overline{INT}$ Low Threshold Voltage | $V_{OL_INT}$ | Sink current = 5mA | -- | -- | 0.4 | V |
| High Level $\overline{INT}$ Leakage Current | $I_{BIAS_INT}$ | Pull high to 1.8V | -- | -- | 1 | μA |
| $\overline{INT}$ Pull Low Time | $t_{INT_PULL_LOW}$ | $\overline{INT}$ pull low time | -- | 256 | -- | μs |
| Output STAT/OTG Low Threshold Voltage | $V_{OL_STAT}$ | Sink current = 5mA | -- | -- | 0.4 | V |
| High Level STAT/OTG Leakage Current | $I_{BIAS_STAT}$ | Pull high to 1.8V | -- | -- | 1 | μA |
| Input STAT/OTG High Threshold Voltage | $V_{IH_OTG}$ | STAT configure to OTG pin | 1.3 | -- | -- | V |
| Input STAT/OTG LOW Threshold Voltage | $V_{IL_OTG}$ | STAT configure to OTG pin | -- | -- | 0.4 | V |
| **D+/D- Detection** | | | | | | |
| Data Detect Voltage | $V_{DAT_REF}$ | For primary/secondary detection | 340 | 375 | 400 | mV |
| D+ Current Sink | $I_{D+_ISNK}$ | $V_{D+}$ = 500mV | 25 | 45 | 65 | μA |
| D- Current Sink | $I_{D-_ISNK}$ | $V_{D-}$ = 500mV | 25 | 45 | 65 | μA |
| D+/ D- Leakage Current | $I_{D+D-_LKG}$ | HIZ mode | –1 | -- | 1 | μA |
| D+ Logic Threshold | $V_{LGC}$ | $V_{D+}$ rising | 800 | 900 | 1000 | mV |
| D+ Current Source | $I_{D+_SRC}$ | $V_{D+}$ = 200mV | 7 | 10 | 13 | μA |
| D+ Voltage Source | $V_{D+_SRC}$ | | 600 | 650 | 700 | mV |
| D- Voltage Source | $V_{D-_SRC}$ | | 600 | 650 | 700 | mV |
| D+ Pulldown for Connection Check | $R_{D+_19K}$ | | 16 | 20 | 24 | kΩ |
| D- Pulldown for Connection Check | $R_{D-_19K}$ | | 16 | 20 | 24 | kΩ |

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|---|---|---|---|---|---|---|
| D+D- Threshold for Non-Standard Adapter (0.9V) | $V_{D+D-_0P9}$ | | 0.81 | 0.9 | 0.99 | V |
| D+D- Threshold for Non-Standard Adapter (1.5V) | $V_{D+D-_1P5}$ | | 1.4 | 1.5 | 1.6 | V |
| D+D- Threshold for Non-Standard Adapter (2.3V) | $V_{D+D-_2P3}$ | | 2.2 | 2.3 | 2.4 | V |
| D+D- Threshold for CDP | $V_{D+D-_CDP}$ | For host mode, CDP | 1.8 | 2 | 2.2 | V |
| Across D+/D- Resistance in DCP | $R_{DCP}$ | For host mode, DCP | -- | 50 | 150 | Ω |
| **ADC Measurement** | | | | | | |
| Effective Resolution | $ADC_{RES}$ | ADC 16 bits | 14 | 15 | -- | bits |
| Conversion-Time | $t_{ADC_CONV}$ | | -- | 3.6 | -- | ms |
| ADC VBUS Voltage Reading Range | $V_{BUS_ADC_RANGE}$ | | 0 | -- | 30 | V |
| ADC VBUS Voltage Reading Resolution | $V_{BUS_ADC_RES}$ | LSB | -- | 1 | -- | mV |
| ADC VBUS Voltage Reading Accuracy | $V_{BUS_ADC_ACC}$ | $V_{BUS}$ = 3.6V to 24V | –100 | -- | 100 | mV |
| ADC IBUS Current Reading Range | $I_{BUS_ADC_RANGE}$ | | 0 | -- | 5 | A |
| ADC IBUS Current Reading Resolution | $I_{BUS_ADC_RES}$ | LSB | -- | 1 | -- | mA |
| ADC IBUS Current Reading Accuracy | $I_{BUS_ADC_ACC}$ | $I_{BUS}$ = 0.5A to 1A | –100 | -- | 100 | mA |
| ADC VAC1 Voltage Reading Range | $V_{AC1_ADC_RANGE}$ | | 0 | -- | 30 | V |
| ADC VAC1 Voltage Reading Resolution | $V_{AC1_ADC_RES}$ | LSB | -- | 1 | -- | mV |
| ADC VAC1 Voltage Reading Accuracy | $V_{AC1_ADC_ACC}$ | $V_{AC1}$ = 3.6V to 24V | –100 | -- | 100 | mV |
| ADC VAC2 Voltage Reading Range | $V_{AC2_ADC_RANGE}$ | | 0 | -- | 30 | V |
| ADC VAC2 Voltage Reading Resolution | $V_{AC2_ADC_RES}$ | LSB | -- | 1 | -- | mV |
| ADC VAC2 Voltage Reading Accuracy | $V_{AC2_ADC_ACC}$ | $V_{AC2}$ = 3.6V to 24V | –100 | -- | 100 | mV |
| ADC VSYS Voltage Reading Range | $V_{SYS_ADC_RANGE}$ | | 0 | -- | 23 | V |
| ADC VSYS Voltage Reading Resolution | $V_{SYS_ADC_RES}$ | LSB | -- | 1 | -- | mV |
| ADC VSYS Voltage Reading Accuracy | $V_{SYS_ADC_ACC}$ | $V_{SYS}$ = 2.5V to 13V | –75 | -- | 75 | mV |
| ADC VBAT Voltage Reading Range | $V_{BAT_ADC_RANGE}$ | | 0 | -- | 20 | V |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ADC VBAT Voltage Reading Resolution | $V_{BAT_ADC_RES}$ | LSB | -- | 1 | -- | mV |
| ADC VBAT Voltage Reading Accuracy | $V_{BAT_ADC_ACC}$ | $V_{BAT}$ = 2V to 12.6V | –100 | -- | 100 | mV |
| ADC IBAT Current Reading Range | $I_{BAT_ADC_RANGE}$ | | 0 | -- | 8 | A |
| ADC IBAT Current Reading Resolution | $I_{BAT_ADC_RES}$ | LSB | -- | 1 | -- | mA |
| ADC IBAT Current Reading Accuracy | $I_{BAT_ADC_ACC}$ | $I_{BAT}$ = 0.5A to 1A | –100 | -- | 100 | mA |
| ADC TS Reading Range | $RATIO_{TS_ADC_RANGE}$ | Ratio for $V_{TS}/V_{REGN}$ | 0 | -- | 99.9 | % |
| ADC TS Reading Resolution | $RATIO_{TS_ADC_RES}$ | LSB | -- | 0.0963 | -- | % |
| ADC TS Reading Accuracy | $RATIO_{TS_ADC_ACC}$ | $V_{TS}$ = 0.1V to 4.7V | –2.7927 | -- | 2.7927 | % |
| ADC Die Temperature Reading Range | $T_{DIE_ADC_RANGE}$ | | –40 | -- | 150 | °C |
| ADC Die Temperature Reading Resolution | $T_{DIE_ADC_RANGE}$ | LSB | -- | 1 | -- | °C |
| ADC Die Temperature Reading Accuracy | $T_{DIE_ADC_ACC}$ | $T_J$ = 0°C to 85°C (Note 7) | –5 | -- | 5 | °C |
| ADC D+ Voltage Reading Range | $V_{D+_ADC_RANGE}$ | | 0 | -- | 3600 | mV |
| ADC D+ Voltage Reading Resolution | $V_{D+_ADC_RES}$ | LSB | -- | 1 | -- | mV |
| ADC D+ Voltage Reading Accuracy | $V_{D+_ADC_ACC}$ | D+ = 0V to 3.6V, HZ mode | –18 | -- | 18 | mV |
| ADC D- Voltage Reading Range | $V_{D-_ADC_RANGE}$ | | 0 | -- | 3600 | mV |
| ADC D- Voltage Reading Resolution | $V_{D-_ADC_RES}$ | LSB | -- | 1 | -- | mV |
| ADC D- Voltage Reading Accuracy | $V_{D-_ADC_ACC}$ | D- = 0V to 3.6V, HZ mode | –18 | -- | 18 | mV |
| **Timing Requirements** | | | | | | |
| Charge Safe Timer for Trickle Charge | $t_{TRI_SAFE_TMR}$ | | 0.9 | 1 | 1.1 | hr |
| Charge Safe Timer for Pre-Charge | $t_{PRE_SAFE_TMR}$ | PRECHG_TMR = 2hr | 1.8 | 2 | 2.2 | hr |
| Charge Safe Timer for Fast Charge | $t_{CHG_SAFE_TMR}$ | FASTCHG_TMR = 5hr | 4.5 | 5 | 5.5 | hr |
| | | FASTCHG_TMR = 8hr | 7.2 | 8 | 8.8 | |
| | | FASTCHG_TMR = 12hr | 10.8 | 12 | 13.2 | |
| | | FASTCHG_TMR = 24hr | 21.6 | 24 | 26.4 | |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Back-Ground Charge Timer | $t_{BG_CHG_TMR}$ | BG_CHG_TMR = 15min | 12 | 15 | 18 | min |
| | | BG_CHG_TMR = 30min | 24 | 30 | 36 | |
| | | BG_CHG_TMR = 45min | 36 | 45 | 54 | |
| **Watchdog Timer** | | | | | | |
| Watchdog Timer | $t_{WDT}$ | WATCHDOG = 160s | 144 | 160 | 176 | s |

**Note 2**. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 3**. $\theta_{JA}$ is measured under natural convection (still air) at $T_A$ = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. $\theta_{JC}$ is measured at the exposed pad of the package.

**Note 4**. Devices are ESD sensitive. Handling precautions are recommended.

**Note 5**. The device is not guaranteed to function outside its operating conditions.

**Note 6**. Maximum output current for ISYS recommend to set switching frequency on 1MHz.

**Note 7**. Specification is guaranteed by design and/or correlation with statistical process control.

**Note 8**. Refer to MIVR section in the Application Information for detailed descriptions.

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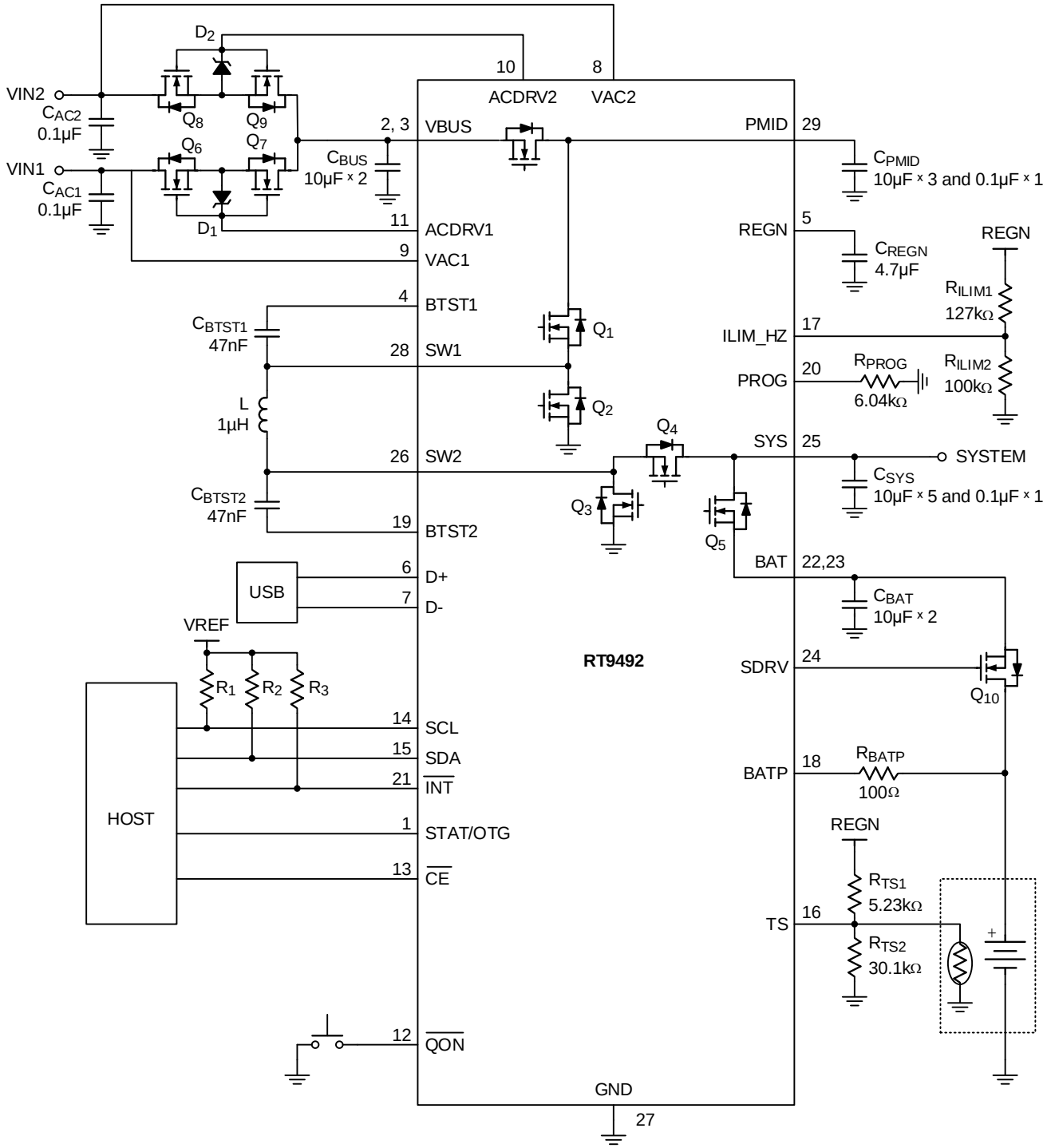
## Typical Application Circuit

### RT9492 with Dual input and Ship FET

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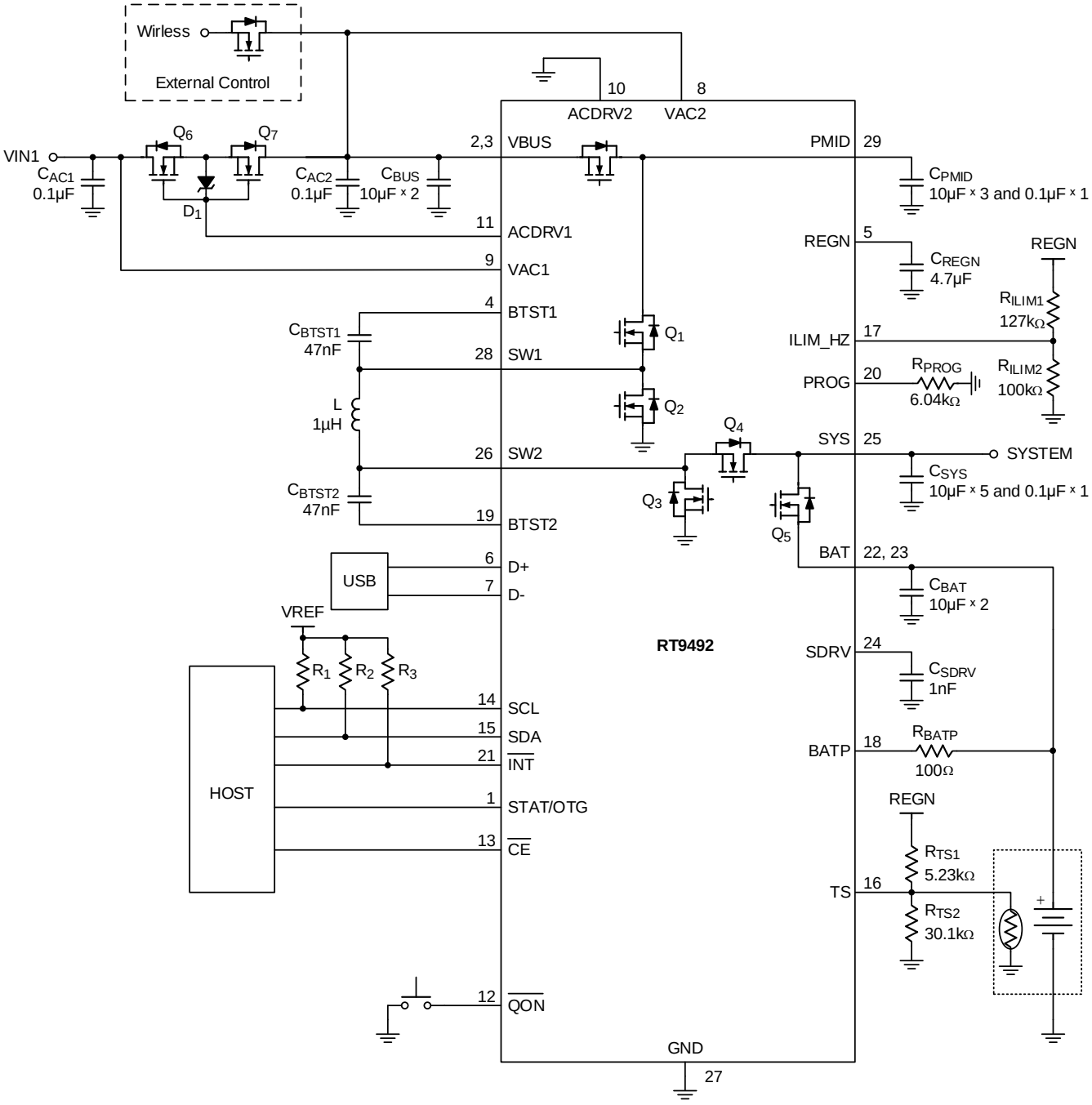
**RT9492 with Single ACRBFET and No Ship FET**

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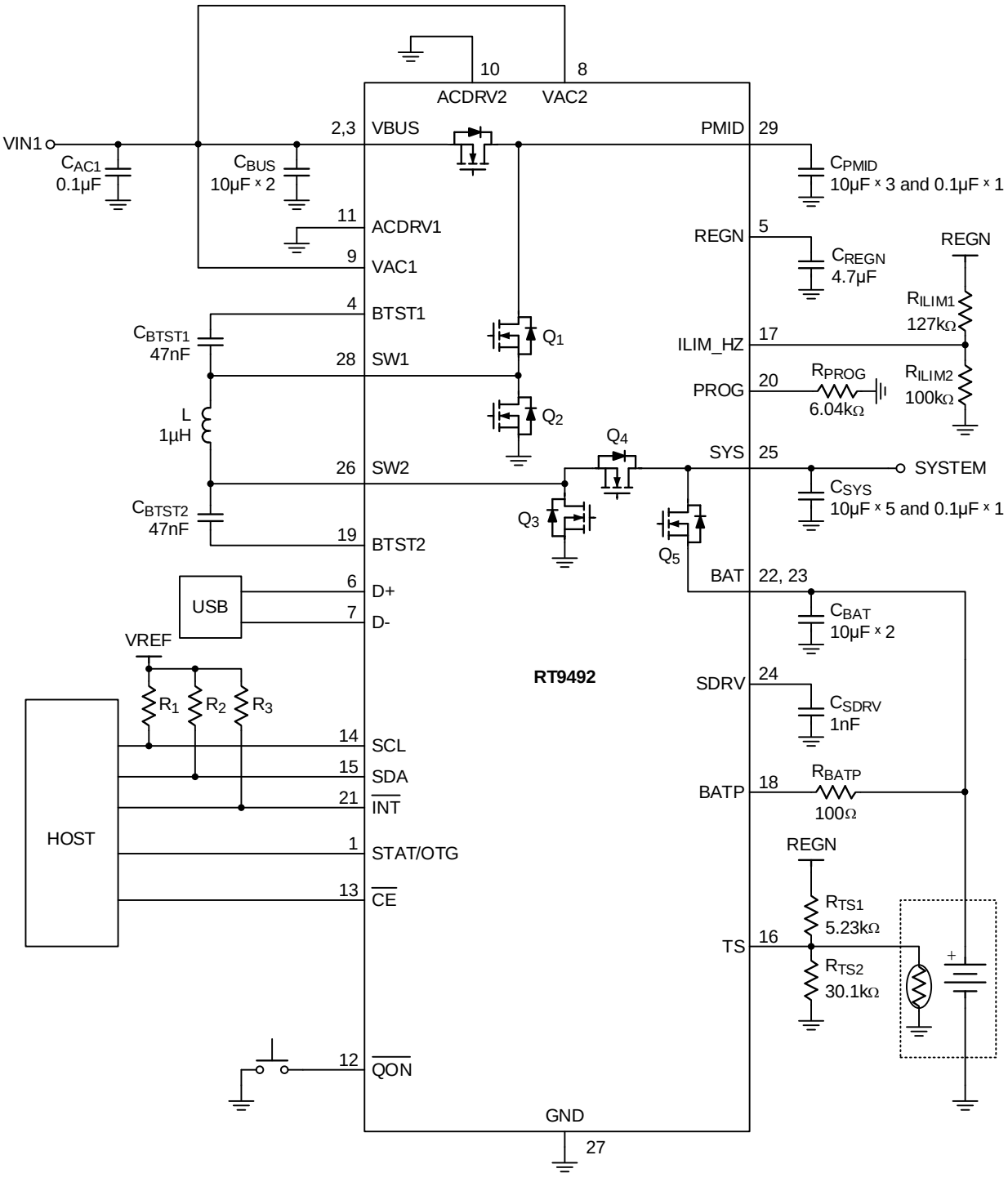
**RT9492 with Single Input and No Ship FET**

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**Below are recommended components information**

| Name | Part Number | Description | Package | Manufacturer |
|---|---|---|---|---|
| $C_{AC1}$ | 0402B104K500CT | 0.1μF/50V/X7R | 0402 | WALSIN |
| $C_{AC2}$ | 0402B104K500CT | 0.1μF/50V/X7R | 0402 | WALSIN |
| $C_{BUS}$ | GRM188R6YA106MA73 | 10μF/35V/X5R | 0603 | MURATA |
| $C_{PMID}$ | GRM188R6YA106MA73 | 10μF/35V/X5R | 0603 | MURATA |
| $C_{PMID}$ | 0402B104K500CT | 0.1μF/50V/X7R | 0402 | WALSIN |
| $C_{BTST1}$ | GRM033R61C473KE84 | 47nF/16V/X5R | 0201 | MURATA |
| $C_{BTST2}$ | GRM033R61C473KE84 | 47nF/16V/X5R | 0201 | MURATA |
| $C_{SYS}$ | GRM188R61E106MA73 | 10μF/25V/X5R | 0603 | MURATA |
| $C_{SYS}$ | 0402B104K500CT | 0.1μF/50V/X7R | 0402 | WALSIN |
| $C_{BAT}$ | GRM188R61E106MA73 | 10μF/25V/X5R | 0603 | MURATA |
| $C_{REGN}$ | GRM155R60J475ME47D | 4.7μF/6.3V/X5R | 0402 | MURATA |
| L | PIMB063T-1R0MS-68 | 1μH/20%/6.7mΩ | 6.8x7.3x3.0mm | CYNTEC |
| | PIMB063T-2R2MS-68 | 2.2μH/20%/ 13.5mΩ | 6.8x7.3x3.0mm | CYNTEC |
| Q6, Q7, Q8, Q9 | AONR36366 | N-MOSFET | DFN 3x3 EP | ALPHA and OMEGA |
| Q10 | AON7528 | N-MOSFET | DFN 3.3x3.3 EP | ALPHA and OMEGA |

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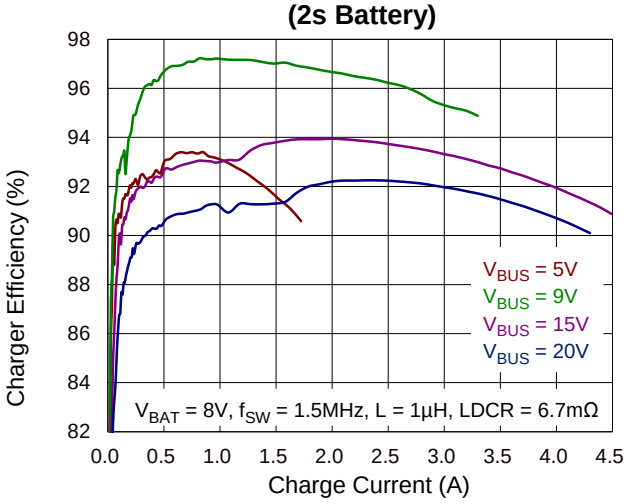
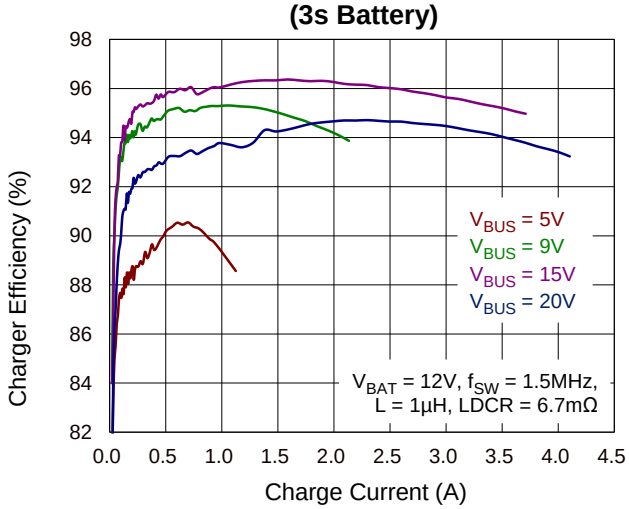
## Typical Operating Characteristics

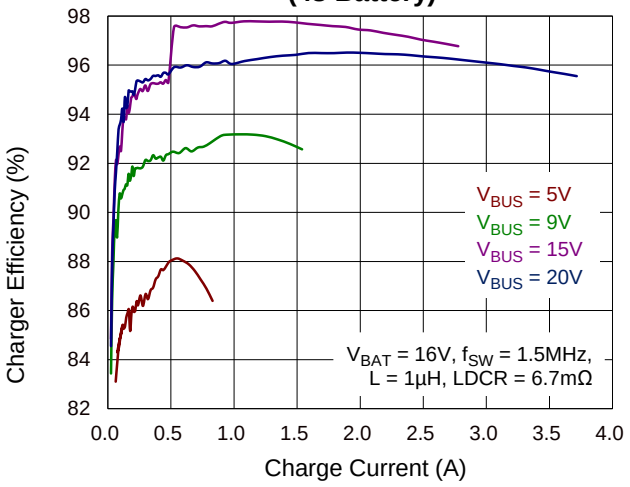
**Charger Efficiency vs. Charge Current (2s Battery)**



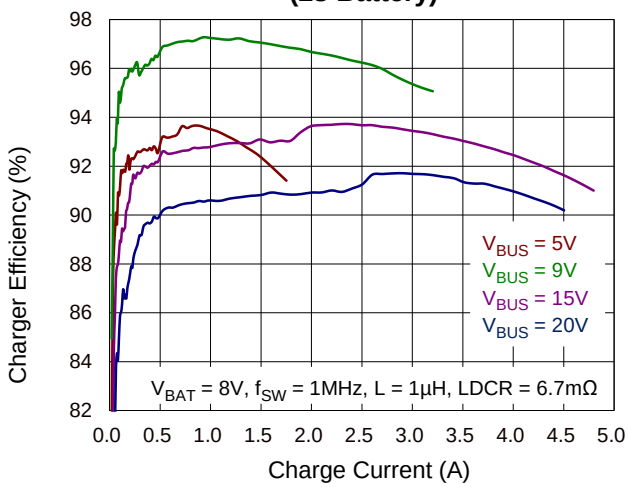

**Charger Efficiency vs. Charge Current (3s Battery)**



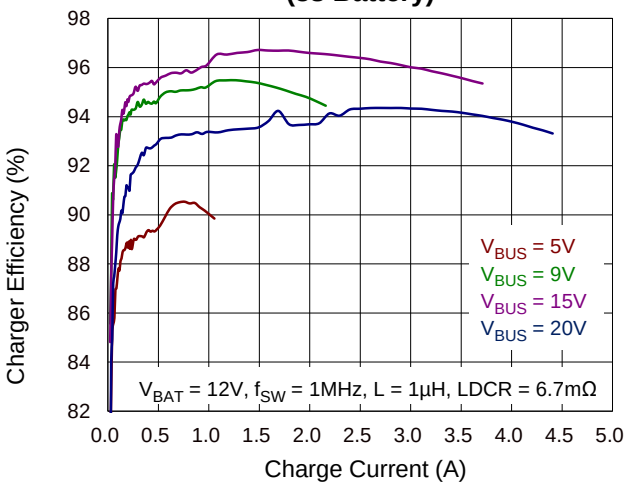

**Charger Efficiency vs. Charge Current (4s Battery)**



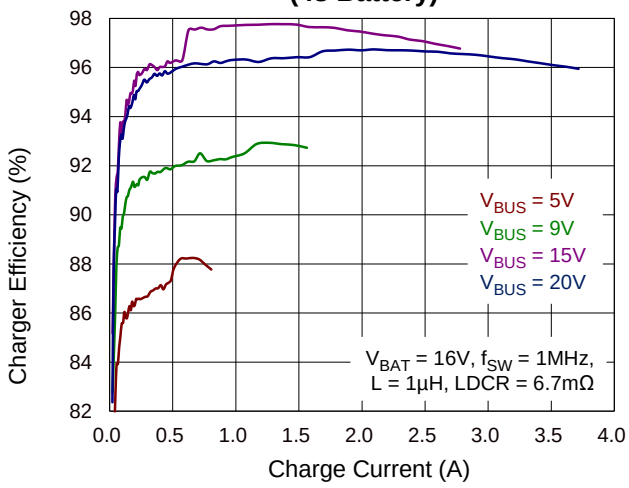

**Charger Efficiency vs. Charge Current (2s Battery)**




**Charger Efficiency vs. Charge Current (3s Battery)**




**Charger Efficiency vs. Charge Current (4s Battery)**

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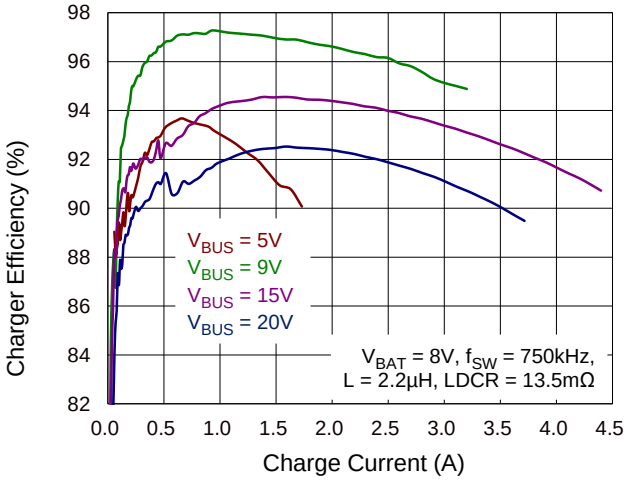
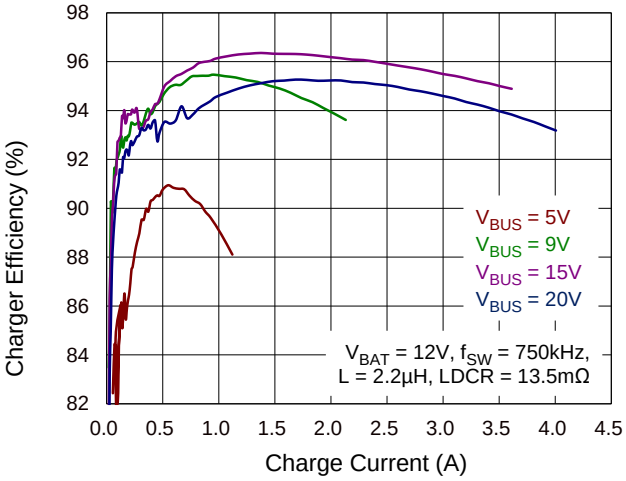
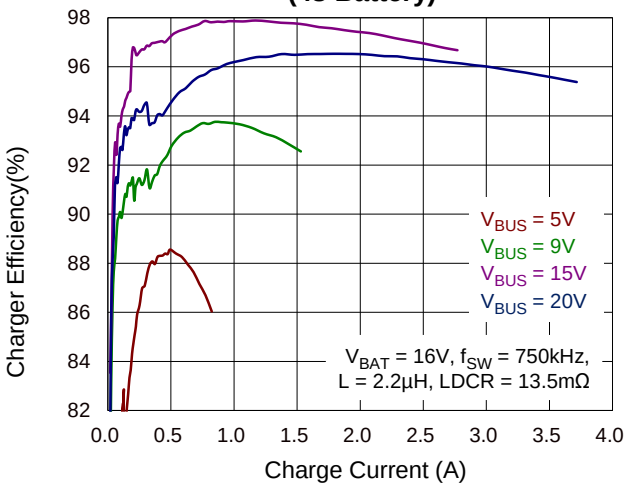
### Charger Efficiency vs. Charge Current (2s Battery)



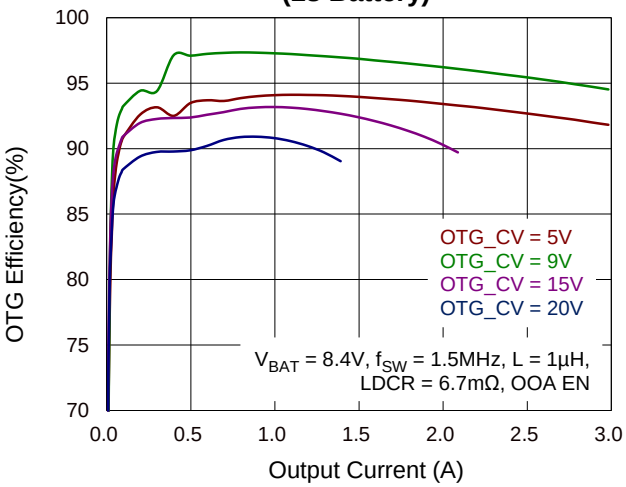

### Charger Efficiency vs. Charge Current (3s Battery)



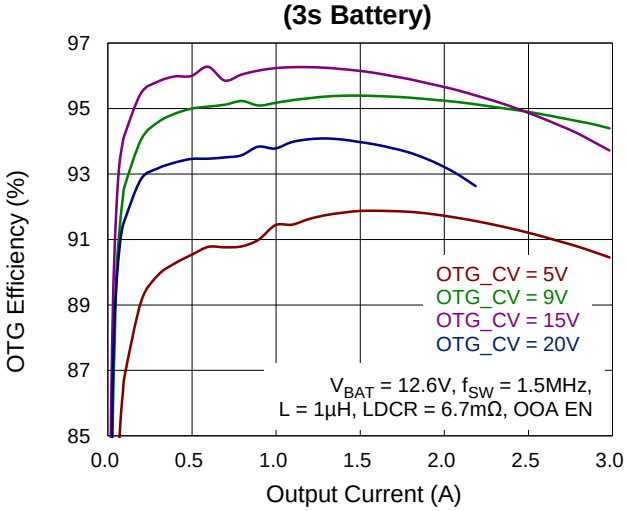

### Charger Efficiency vs. Charge Current (4s Battery)



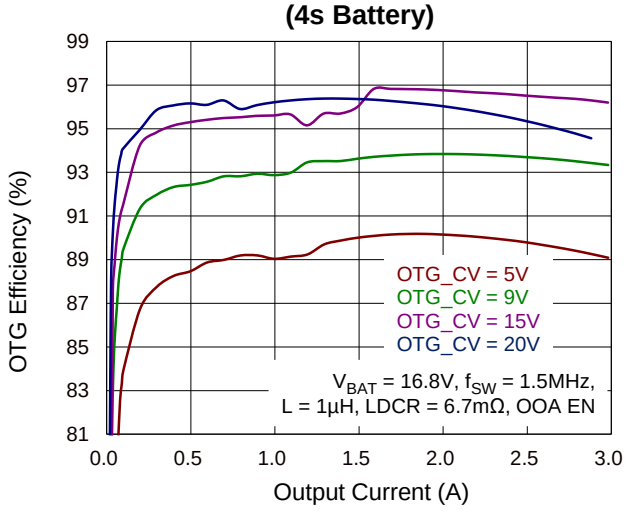

### OTG Efficiency vs. Output Current (2s Battery)




### OTG Efficiency vs. Output Current (3s Battery)




### OTG Efficiency vs. Output Current (4s Battery)

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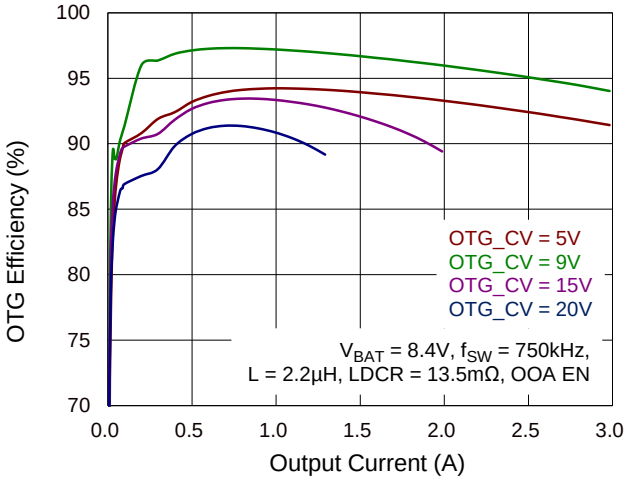
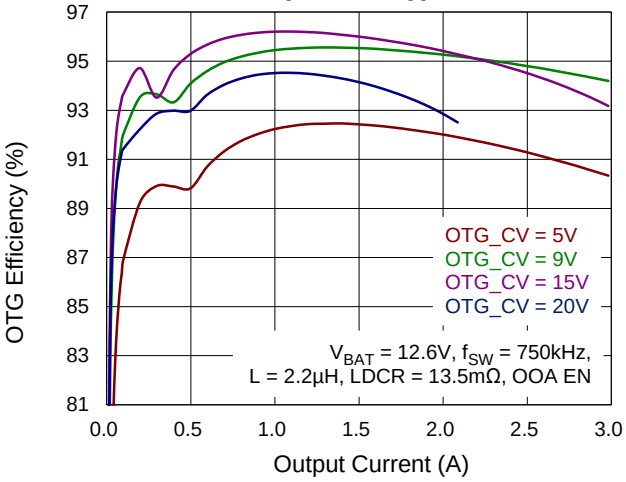
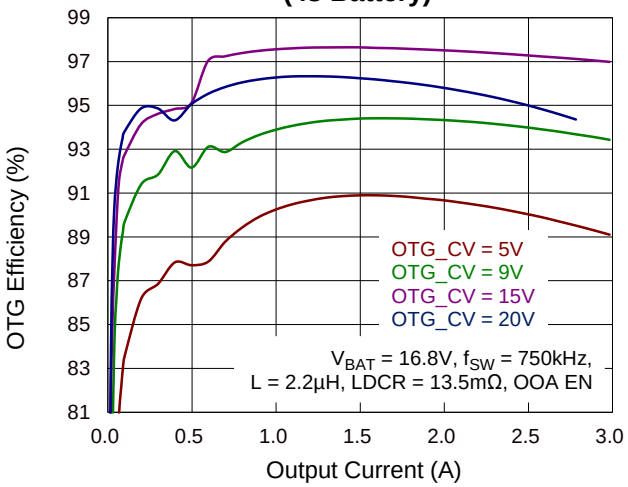
**OTG Efficiency vs. Output Current (2s Battery)**



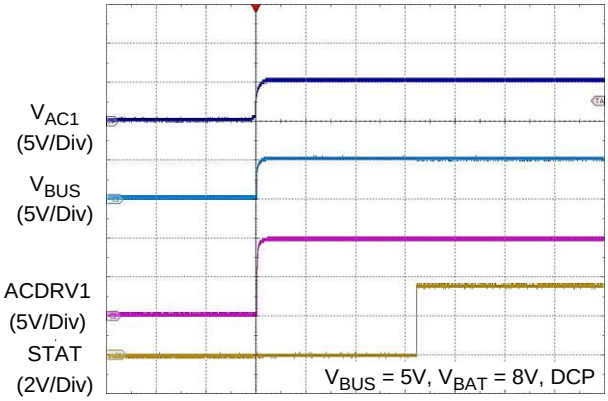

**OTG Efficiency vs. Output Current (3s Battery)**



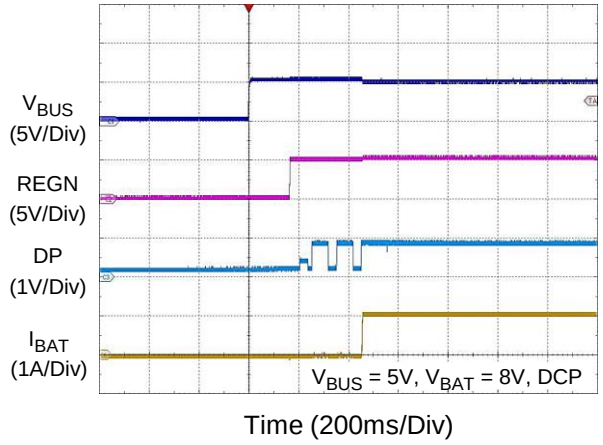

**OTG Efficiency vs. Output Current (4s Battery)**



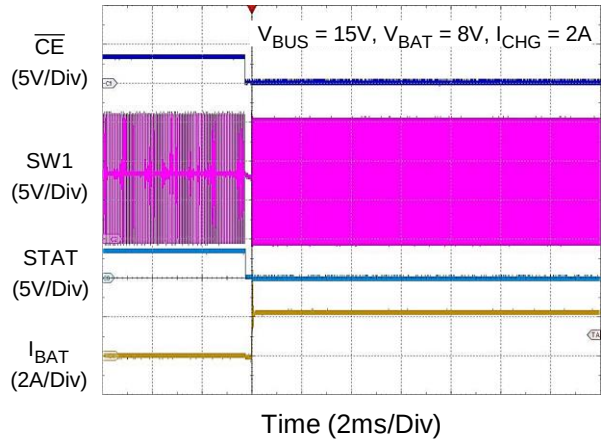

**Power-UP with AC_RB1, VAC1 Plug in**




**Power-UP with Single Input, VBUS Plug in**




**Charger Enabled**

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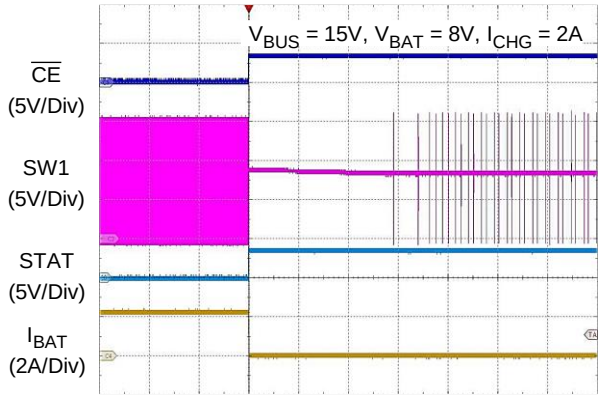
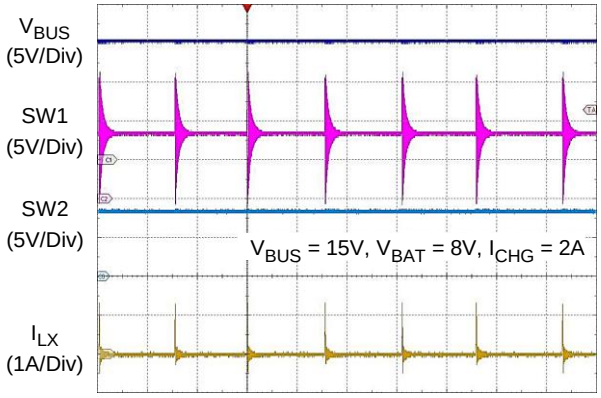
### Charger Disabled



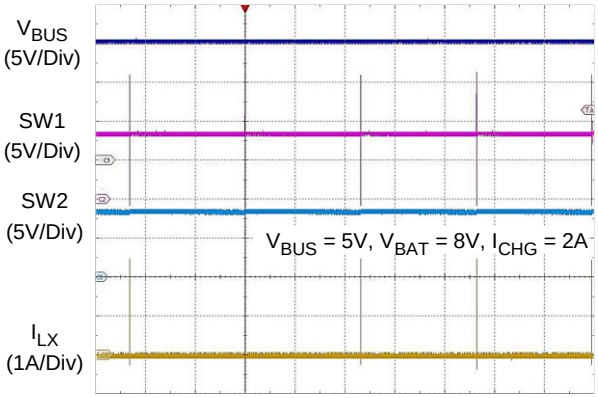

Time (2ms/Div)

### Charger Disabled, OOA Enabled



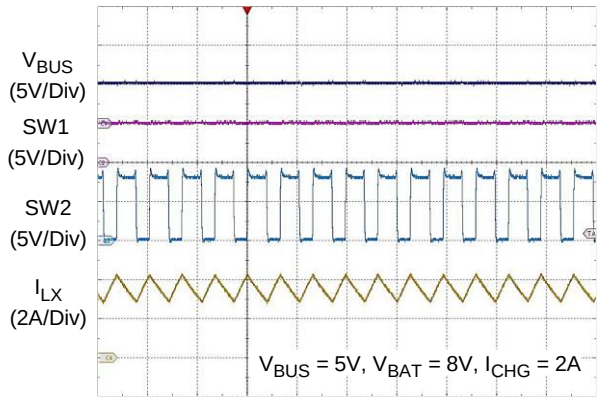

Time (20μs/Div)

### Charger Disabled, OOA Disabled



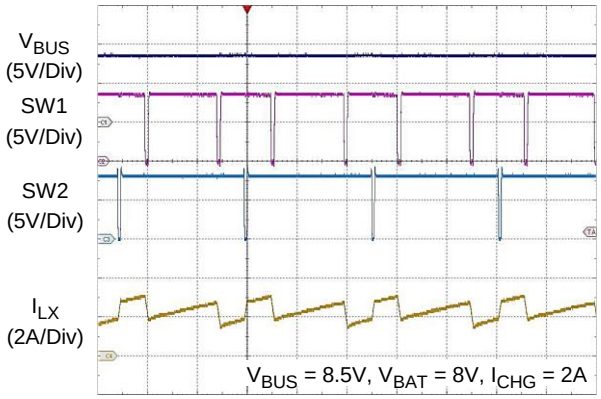

Time (1ms/Div)

### Boost Mode, Charger Enabled



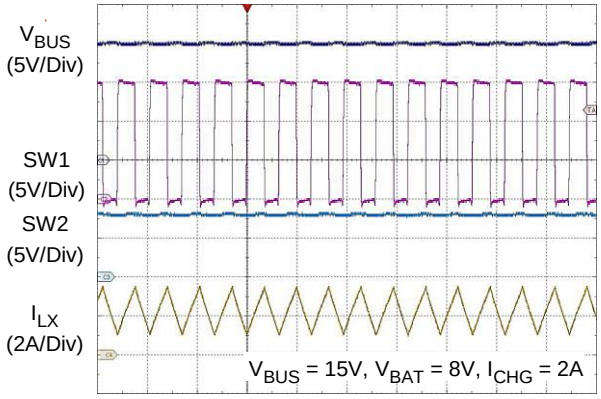

Time (1μs/Div)

### Buck-Boost Mode, Charger Enabled




Time (2μs/Div)

### Buck Mode, Charger Enabled




Time (1μs/Div)

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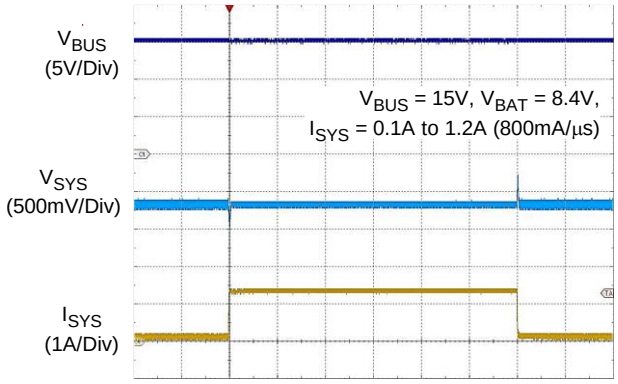
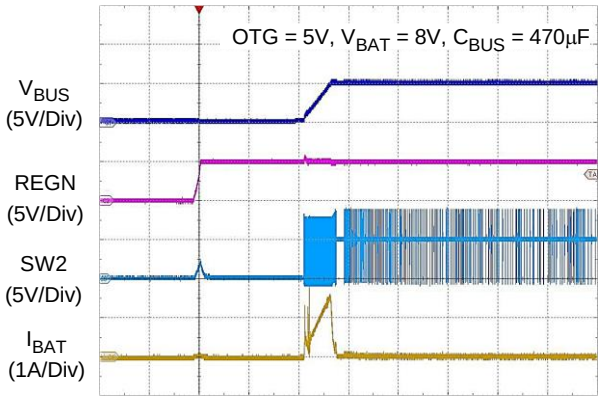
### System Load Transient, Charger Disabled



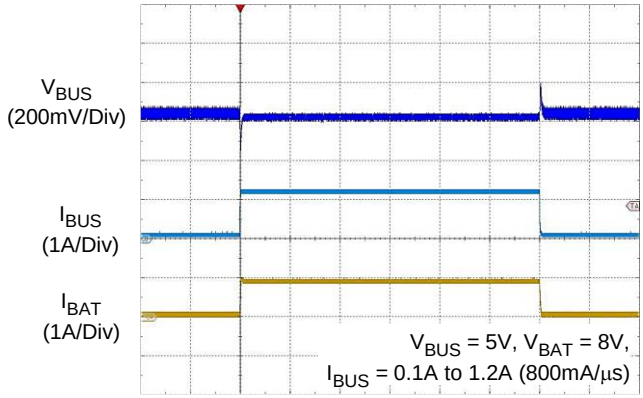

Time (1ms/Div)

### OTG Start-Up



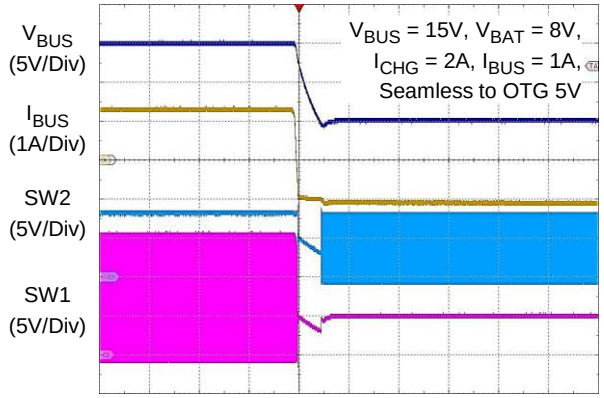

Time (2ms/Div)

### OTG Load Transient



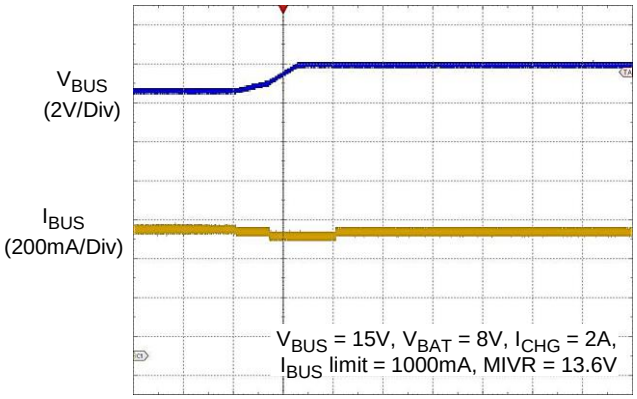

Time (1ms/Div)

### Seamless




Time (200μs/Div)

### AICC Enabled




Time (50ms/Div)

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## Register Description

I²C Slave Address: 1010011 (53H)

R: Read only

R/W: Read and write

RWS: Read and write, also automatically set by particular condition

RWC: Read and write, also automatically cleared by particular condition

RWSC: Read and write, also automatically set/cleared by particular condition

Register Address: 0x00, Register Name: SYS_MIN REGU

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:6 | RESERVED | 00 | N | N | R | Reserved |
| 5:0 | VSYSMIN | NA | N | Y | RWSC | During POR, the device reads the resistance on PROG pin, to identify the default battery cell count and determine the default VSYSMIN, change REG0x0A[7:6] also change default value<br>000000: 2.5V<br>000001: 2.75V<br>…<br>000100: 3.5V<br>...<br>010010: 7V (2s)<br>…<br>011010: 9V (3s)<br>…<br>100110: 12V (4s)<br>…<br>110101: 15.75V<br>110110 to 111111: 16V |

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Register Address: 0x01, Register Name: VCHG_CTRL

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:11 | RESERVED | 00000 | N | N | R | Reserved |
| 10:0 | VBAT_REG | NA | N | Y | RWSC | During POR, the device reads the resistance on PROG pin, to identify the default battery cell count and determine the default power-on battery voltage, change REG0x0A[7:6] also change default value<br>00111110100: 5V<br>…<br>01101001000: 8.4V (2s)<br>…<br>10011101100: 12.6V (3s)<br>…<br>11010010000: 16.8V (4s)<br>…<br>11101010111: 18.79V<br>11101011000 to 11111111111: 18.8V |

Register Address: 0x03, Register Name: ICHG_CTRL

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:9 | RESERVED | 0000000 | N | N | R | Reserved |
| 8:0 | ICHG_CTRL | NA | Y | Y | RWSC | During POR, the device reads the resistance on PROG pin, to identify the default battery cell count and determine the default power-on battery charging current, change REG0x0A[7:6] also change default value<br>0000000000 to 0000001110: Reserved<br>000001111: 0.15A<br>…<br>001100100: 1A (3s, 4s)<br>…<br>011001000: 2A (2s)<br>…<br>111110011: 4.99A<br>111110100 to 111111111: 5A |

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Register Address: 0x05, Register Name: MIVR_CTRL

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:0 | VMIVR | 00100100 | N | N | RWS | MIVR is set to the value based on the VBUS measurement when the adapter plugs in and AUTO_MIVR = 1<br>00000000 to 00100100: 3.6V (Default)<br>00100101: 3.7V<br>…<br>01101010: 10.6V<br>…<br>11011011: 21.9V<br>11011100 to 11111111: 22V |

Register Address: 0x06, Register Name: AICR_CTRL

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:9 | RESERVED | 0000000 | N | N | R | Reserved |
| 8:0 | IAICR | 10010 1100 | N | Y | RWSC | Based on D+/D- detection results, if AUTO_AICR = 1<br>000000000 to 000001010: 100mA<br>000001011: 110mA<br>…<br>000110010: 500mA<br>…<br>100101100: 3000mA (Default)<br>…<br>101001010 to 111111111: 3300mA |

Register Address: 0x08, Register Name: PRE_CHG

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:6 | VPRE_CHG | 11 | N | Y | R/W | Pre-charge voltage threshold from<br>00: 15%*VBAT_REG<br>01: 62%*VBAT_REG<br>10: 66.5%*VBAT_REG<br>11: 71.5%*VBAT_REG (Default) |
| 5:0 | IPRE_CHG | 000011 | Y | Y | R/W | Pre-charge current<br>000000 to 000010: Reserved<br>000011: 0.12A (Default)<br>…<br>110001: 1.96A<br>110010 to 111111: 2A |

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Register Address: 0x09, Register Name: EOC_CTRL

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | RST_ALL | 0 | N | Y | RWC | All registers and logic reset bit.<br>0: No action (Default)<br>1: Reset all registers and logic.<br>Back to 0 after register and logic reset |
| 6 | REG_RST | 0 | N | Y | RWC | Reset registers to default values and reset timer<br>0: No action (Default)<br>1: Reset register and safety timer<br>Back to 0 after register reset |
| 5 | Reserved | 0 | N | N | R | Reserved |
| 4:0 | IEOC | 00101 | Y | Y | R/W | End-of-charge current<br>00000 to 00010: Reserved<br>00011: 0.12A<br>00100: 0.16A<br>00101: 0.2A (Default)<br>…<br>11000: 0.96A<br>11001 to 11111: 1A |

Register Address: 0x0A, Register Name: RECHG

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:6 | BATTERY_CELL | NA | N | N | R/W | After POR, the device reads the PROG pin resistance to determine the battery cell.<br>01: 2s<br>10: 3s<br>11: 4s<br>This Bit is only for 01, 10,11 setting. |
| 5:4 | TRECHG | 10 | Y | Y | R/W | Re-charge deglitch time<br>00: 64ms<br>01: 256ms<br>10: 1024ms (Default)<br>11: 2048ms |
| 3:0 | VRECHG | 0011 | Y | Y | R/W | Re-charge voltage threshold<br>0000: 50mV<br>0001: 100mV<br>0010: 150mV<br>0011: 200mV (Default)<br>…<br>1110: 750mV<br>1111: 800mV |

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Register Address: 0x0B, Register Name: VOTG_REGU

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:11 | RESERVED | 00000 | N | N | R | Reserved |
| 10:0 | VOTG | 0001101 1100 | Y | Y | R/W | OTG voltage regulation<br>00000000000: 2.8V<br>00000000001: 2.81V<br>…<br>00011011100: 5V (Default)<br>…<br>11101111111: 21.99V<br>11110000000 to 11111111111: 22V |

Register Address: 0x0D, Register Name: IOTG_REGU

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | PRECHG_ TMR | 0 | Y | Y | R/W | Pre-charge safe timer<br>0: 2 hr (Default)<br>1: 0.5 hrs |
| 6:0 | IOTG | 1001011 | Y | Y | R/W | OTG current limit<br>0000000 to 0000011: 0.12A<br>0000100: 0.16A<br>…<br>1001011: 3A (Default)<br>…<br>1010010: 3.28A<br>1010011 to 1111111: 3.32A |

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Register Address: 0x0E, Register Name: SAFETY_TMR_CTRL

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:6 | BG_CHG_TMR | 00 | Y | Y | R/W | EOC back-ground charge timer<br>00: Disabled (Default)<br>01: 15 mins<br>10: 30 mins<br>11: 45 mins |
| 5 | EN_TRICHG_TMR | 1 | Y | Y | R/W | Trickle charge safe timer enable<br>0: Disabled<br>1: Enabled (Default) |
| 4 | EN_PRECHG_TMR | 1 | Y | Y | R/W | Pre-charge safe timer enable<br>0: Disabled<br>1: Enabled (Default) |
| 3 | EN_FASTCHG_TMR | 1 | Y | Y | R/W | Fast-charge safe timer enable<br>0: Disabled<br>1: Enabled (Default) |
| 2:1 | FASTCHG_TMR | 10 | Y | Y | R/W | Fast-charge safe timer<br>00: 5 hr<br>01: 8 hr<br>10: 12 hr (Default)<br>11: 24 hr |
| 0 | TMR2X_EN | 1 | Y | Y | R/W | Double charge safe timer during MIVR, AICR, thermal regulation, and JEITA reduce ICHG<br>0: Disable 2x extended charge safe timer<br>1: Enable 2x extended charge safe timer (Default) |

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Register Address: 0x0F, Register Name: CHG_CTRL 0

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | EN_AUTO_ IBATDIS | 1 | N | Y | R/W | Enable the battery discharging during the battery OVP fault<br>0: No action when VBAT during VBAT_OVP<br>1: Apply a discharging resistance on VBAT during VBAT_OVP (Default) |
| 6 | FORCE_ IBATDIS | 0 | N | Y | R/W | Force a battery discharging resistance<br>0: No action (Default)<br>1: Force a discharging resistance on BAT |
| 5 | EN_CHG | 1 | Y | Y | R/W | Charger Enable<br>0: Disable charge<br>1: Enable charge (Default) |
| 4 | EN_AICC | 0 | N | Y | R/W | 0: Disable AICC function (Default)<br>1: Enable AICC function |
| 3 | FORCE_AICC | 0 | Y | Y | RWSC | 0: No action (Default)<br>1: Force AICC function<br>Back to 0 after AICC done |
| 2 | EN_HZ | 0 | N | Y | RWSC | Enable HZ mode<br>0: Disable (Default)<br>1: Enable<br>Back to 0 when VAC/VBUS prescent |
| 1 | EN_TE | 1 | Y | Y | R/W | Charge current termination<br>0: Disable<br>1: Enable (Default) |
| 0 | RESERVED | 0 | N | N | R | Reserved |

Register Address: 0x10, Register Name: CHG_CTRL 1

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:6 | RESERVED | 00 | N | N | R | Reserved |
| 5:4 | VAC_OVP | 00 | N | Y | R/W | VAC1/VAC2_OVP thresholds<br>00: 26V (Default)<br>01: 18V<br>10: 12V<br>11: 7V |
| 3 | WD_RST | 0 | Y | Y | RWSC | Watch dog timer reset<br>0: No action (Default)<br>1: Reset<br>Back to 0 after WDT resets |
| 2:0 | WATCHDOG | 101 | N | Y | R/W | Watchdog timer settings<br>000: Disable<br>001: 0.5s<br>010: 1s<br>011: 2s<br>100: 20s<br>101: 40s (Default)<br>110: 80s<br>111: 160s |

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Register Address: 0x11, Register Name: CHG_CTRL 2

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | FORCE_ DPDM_DET_ EN | 0 | Y | Y | RWSC | Force D+/D- detection<br>0: No action (Default)<br>1: Force D+D- detection<br>Back to 0 while D+D- detect done |
| 6 | BC12_EN | 1 | Y | Y | R/W | 0: Disable BC1.2 detection<br>1: Enable BC1.2 detection (Default) |
| 5:4 | RESERVED | 00 | N | N | R | Reserved |
| 3 | DIS_EOC_ FCCM | 1 | N | Y | R/W | Enable FCCM for EOC during TD_EOC<br>0: Enable EOC FCCM<br>1: Disable EOC FCCM (Default) |
| 2:1 | SDRV_CTRL | 00 | N | Y | RWSC | SHIP FET gate driver control mode<br>00: IDLE (Default)<br>01: Shutdown Mode<br>10: Ship Mode<br>11: System Power Reset<br>Back to 00 when SHIP_FET_PRESENT = 0 or exit Shutdown Mode or exit Ship Mode or finish System Power Reset. Set to Ship mode when SHIP_FET_PRESENT = 1 and trigger IBAT_OCP or VSYS_SHORT |
| 0 | SDRV_DLY | 0 | N | Y | R/W | SHIP FET turn off delay time when SDRV_CTRL not equal to 00<br>0: Add 10s delay time (Default)<br>1: Do NOT add 10s delay time |

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Register Address: 0x12, Register Name: CHG_CTRL 3

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | DIS_ACDRV_EN | 0 | N | N | RWSC | Force both EN_ACDRV1 = 0 and EN_ACDRV2 = 0<br>0: Not Force (Default)<br>1: Force EN_ACDRV1 = 0 and EN_ACDRV2 = 0<br>Clear to 0 when VAC1/VAC2 not present and EN_OTG disable |
| 6 | EN_OTG | 0 | Y | Y | RWSC | OTG mode control<br>0: Disable OTG (Default)<br>1: Enable OTG<br>(Back to 0 when OTG_UVP, OTG_LBP. Set to 1 when SEAMLESS operating) |
| 5:4 | RESERVED | 00 | N | N | R | Reserved |
| 3 | QON_EXIT_SHIP_DLY | 0 | N | Y | R/W | QON pin pull low time to exit ship mode<br>0: 1s (Default)<br>1: 15ms |
| 2 | DIS_LDO | 0 | Y | Y | RWC | Disable BATFET LDO mode in SYSMIN<br>0: Enable BATFET regulation for SYSMIN (Default)<br>1: Disable BATFET regulation<br>(Clear to 0 when power path turned off or VBUS no input) |
| 1 | DIS_OTG_OOA | 0 | Y | Y | R/W | Disable OOA in OTG mode<br>0: Enable OOA function in OTG mode (Default)<br>1: Disable OOA function in OTG mode |
| 0 | DIS_CHG_OOA | 0 | N | Y | R/W | Disable OOA in charge mode<br>0: Enable OOA function in charge mode (Default)<br>1: Disable OOA function in charge mode |

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Register Address: 0x13, Register Name: CHG_CTRL 4

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | EN_ACDRV2 | 0 | N | N | RWSC | Externel ACFET2 gate driver<br>0: Turn off (Default)<br>1: Turn on<br>(Set to 1 when VAC2 prescent, back to 0 after VAC2 not prescent or lock at 0 if there is no external ACFET2) |
| 6 | EN_ACDRV1 | 0 | N | N | RWSC | Externel ACFET1 gate driver<br>0: Turn off (Default)<br>1: Turn on<br>(Set to 1 when VAC1 prescent, back to 0 after VAC1 not prescent or lock at 0 if there is no external ACFET1) |
| 5 | PWM_FREQ | NA | N | N | RWSC | Switching frequency selection, after POR, default value is based on the PROG pin<br>0: 1.5MHz<br>1: 750kHz |
| 4 | DIS_STAT | 0 | Y | Y | R/W | STAT pin output<br>0: Enable STAT pin output (Default)<br>1: Disable STAT pin output |
| 3 | DIS_VSYS_ UVP_HICCUP | 0 | N | Y | R/W | VSYS_UVP hiccup protection.<br>0: Enable VSYS_UVP hiccup protection (Default)<br>1: Disable VSYS_UVP hiccup, converter continue switching |
| 2 | DIS_VOTG_ UVP_HICCUP | 0 | N | Y | R/W | OTG mode VOTG UVP hiccup protection.<br>0: Enable VOTG_UVP hiccup protection (Default)<br>1: Disable VOTG_UVP hiccup, converter continue switching |
| 1 | FORCE_ MIVR_DET | 0 | N | Y | RWC | Force MIVR detection<br>0: No action (Default)<br>1: Force the converter stop switching, and ADC VBUS for MIVR detection<br>(Back to 0 after force MIVR detection done) |
| 0 | EN_IBUS_ OCP | 1 | N | Y | R/W | Enable IBUS_OCP<br>0: Disable<br>1: Enable (Default) |

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Register Address: 0x14, Register Name: CHG_CTRL 5

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | SHIP_FET_ PRESENT | 0 | N | N | R/W | The user has to set this bit based on whether a SHIP FET is used or not.<br>0: No external SHIP FET (Default)<br>1: Use external SHIP FET |
| 6:5 | RESERVED | 00 | N | N | R | Reserved |
| 4:3 | IBAT_REG | 10 | Y | Y | RWC | Battery discharging current regulation during OTG<br>00: 3A<br>01: 4A<br>10: 5A (Default)<br>11: Disable<br>(Back to 10, when THREG_STAT trigger and IBAT_REG = 11) |
| 2 | EN_AICR | 1 | Y | Y | RWC | AICR Loop control<br>0: Disable<br>1: Enable (Default)<br>(Back to 1, when THREG_STAT trigger) |
| 1 | ILIM_HZ_EN | 1 | N | Y | R/W | ILIM_HZ pin current limit setting<br>0: Disable<br>1: Enable (Default) |
| 0 | EN_IBAT_ OCP | 0 | Y | Y | RWSC | Enable the battery discharging current OCP<br>0: Disable (Default)<br>1: Enable<br>(Back to 0 when SHIP_FET_PRESENT = 0) |

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Register Address: 0x16, Register Name: THREG_CTRL

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:6 | THREG | 11 | Y | Y | R/W | Thermal Regulation threshold<br>00: 60°C<br>01: 80°C<br>10: 100°C<br>11: 120°C (Default) |
| 5:4 | TOTP | 00 | Y | Y | R/W | Over Thermal Protection thresholds.<br>00: 150°C (Default)<br>01: 130°C<br>10: 120°C<br>11: 85°C |
| 3 | VBUS_PD_EN | 0 | N | Y | R/W | VBUS pull-down resistor<br>0: Disable (Default)<br>1: Enable |
| 2 | VAC1_PD_EN | 0 | N | Y | R/W | VAC1 pull-down resistor<br>0: Disable (Default)<br>1: Enable |
| 1 | VAC2_PD_EN | 0 | N | Y | R/W | VAC2 pull-down resistor<br>0: Disable (Default)<br>1: Enable |
| 0 | THREG_HYS | 0 | N | Y | R/W | Thermal Regulation Falling Hysteresis<br>0: 10°C (Default)<br>1: 20°C |

Register Address: 0x17, Register Name: JEITA_CTRL 0

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:5 | JEITA_VSET | 011 | Y | Y | R/W | JEITA WARM charge voltage setting<br>000: Stop charging<br>001: Set VBAT_REG to VBAT_REG-800mV<br>010: Set VBAT_REG to VBAT_REG-600mV<br>011: Set VBAT_REG to VBAT_REG-400mV (Default)<br>100: Set VBAT_REG to VBAT_REG-300mV<br>101: Set VBAT_REG to VBAT_REG-200mV<br>110: Set VBAT_REG to VBAT_REG-100mV<br>111: VBAT_REG = Register setting |
| 4:3 | JEITA_ISET_WARM | 11 | Y | Y | R/W | JEITA WARM charge current setting<br>00: Stop charging<br>01: Set ICHG to 25% * ICHG<br>10: Set ICHG to 50% * ICHG<br>11: ICHG = Register setting (Default) |
| 2:1 | JEITA_ISET_COOL | 01 | Y | Y | R/W | JEITA COOL charge current setting<br>00: Stop charging<br>01: Set ICHG to 25% * ICHG (Default)<br>10: Set ICHG to 50% * ICHG<br>11: ICHG = Register setting |
| 0 | RESERVED | 0 | N | N | R | Reserved |

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Register Address: 0x18, Register Name: JEITA_CTRL 1

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:6 | TS_COOL | 01 | Y | Y | R/W | TS COOL temperature threshold<br>00: 71.1% (5°C)<br>01: 68.4% (10°C) (Default)<br>10: 65.5% (15°C)<br>11: 62.4% (20°C) |
| 5:4 | TS_WARM | 01 | Y | Y | R/W | TS WARM temperature threshold<br>00: 48.4% (40°C)<br>01: 44.8% (45°C) (Default)<br>10: 41.2% (50°C)<br>11: 37.7% (55°C) |
| 3:2 | OTG_HOT | 01 | Y | Y | R/W | OTG mode TS HOT temperature threshold<br>00: 37.7% (55°C)<br>01: 34.4% (60°C) (Default)<br>10: 31.3% (65°C)<br>11: Disable |
| 1 | OTG_COLD | 0 | Y | Y | R/W | OTG mode TS COLD temperature threshold<br>0: 80% (−10°C) (Default)<br>1: 77.1% (−20°C) |
| 0 | JEITA_DIS | 0 | Y | Y | R/W | Disable JEITA function<br>0: NOT disable (Default)<br>1: Disable |

Register Address: 0x19, Register Name: AICC_CTRL

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:9 | RESERVED | 0000000 | N | N | R | Reserved |
| 8:0 | IAICC | 000000000 | N | N | R | AICR current limit by Average Input Current Control or ILIM_HZ pin<br>000000000: 0mA (Default)<br>000001010: 100mA<br>000001011: 110mA<br>…<br>000110010: 500mA<br>…<br>100101100: 3000mA<br>…<br>101001010: 3300mA |

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Register Address: 0x1B, Register Name: CHG_STATUS 0

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | AICR_STAT | 0 | N | N | R | AICR status (charge mode) or OTG_CC status (OTG mode)<br>0: Normal (Default)<br>1: In AICR/OTG_CC |
| 6 | MIVR_STAT | 0 | N | N | R | MIVR status (charge mode) or OTG_CV status (OTG mode)<br>0: Normal (Default)<br>1: In MIVR/OTG_CV |
| 5 | WDT_STAT | 0 | N | N | R | Watch dog timer status<br>0: Normal (Default)<br>1: Watch dog timeout |
| 4 | RESERVED | 0 | N | N | R | Reserved |
| 3 | VBUS_GD_RDY_STAT | 0 | N | N | R | VBUS good ready for charge status<br>0: VBUS NOT good ready for charge status (Default)<br>1: VBUS good ready for charge status<br>(Notice: after bad adapter detection, REG_HZ = 0, VBUS_OVP = 0) |
| 2 | VAC2_PG_STAT | 0 | N | N | R | VAC2 power good status<br>0: VAC2 NOT power good (Default)<br>1: VAC2 power good<br>(Notice: above VAC_UVLO threshold, VAC2_OVP = 0) |
| 1 | VAC1_PG_STAT | 0 | N | N | R | VAC1 power good status<br>0: VAC1 NOT power good (Default)<br>1: VAC1 power good<br>(Notice: above VAC_UVLO threshold, VAC1_OVP = 0) |
| 0 | VBUS_PG_STAT | 0 | N | N | R | VBUS power good status<br>0: VBUS NOT power good (Default)<br>1: VBUS power good<br>(Notice: above VBUS_UVLO threshold, HZ = 0, VBUS_OVP = 0) |

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Register Address: 0x1C, Register Name: CHG_STATUS 1

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:5 | CHG_STAT | 000 | N | N | R | Charge status bits<br>000: Not charging (Default)<br>001: Trickle charge<br>010: Pre-charge<br>011: Fast charge (CC mode)<br>100: Fast charge (CV mode)<br>101: IEOC (EOC and TE = 0)<br>110: Back-Ground Charging (EOC and TE = 1 and before BATFET turn off)<br>111: Charge Done (EOC and TE = 1 and BATFET turn off) |
| 4:1 | VBUS_STAT | 0000 | N | N | R | VBUS status bits<br>0000: No input or Input NOT from BC12_EN_CHANNEL (Default)<br>0001: USB SDP (0.5A)<br>0010: USB CDP (1.5A)<br>0011: USB DCP (3.25A)<br>0100: Adjustable DCP<br>0101: NSDP/Unknown (3.25A)<br>0110: Special Adapter (1A/2A/2.1A/2.4A)<br>0111: In OTG mode<br>1000: Not verify adapter/Bad adapter<br>1001: Reserved<br>1010: Reserved<br>1011: Device directly powered from VBUS<br>1100: Reserved<br>1101: Reserved<br>1110: Reserved<br>1111: Reserved |
| 0 | BC12_DONE_STAT | 0 | N | N | R | BC1.2 status bit<br>0: BC1.2 NOT complete (Default)<br>1: BC1.2 done |

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Register Address: 0x1D, Register Name: CHG_STATUS 2

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:6 | AICC_STAT | 00 | N | N | R | Average input current control status<br>00: AICC disabled (Default)<br>01: AICC optimization in progress<br>10: Maximum input current detected<br>11: Reserved |
| 5 | CDP_PD_STAT | 0 | N | N | R | CDP primary detection start<br>0: CDP primary detection does not start (Default)<br>1: CDP primary detection started<br>(Notice: This bit will be updated when HOST mode is changed.) |
| 4 | CDP_DONE_STAT | 0 | N | N | R | CDP flow done<br>0: No CDP flow (Default)<br>1: CDP flow done.<br>(Notice: This bit will be updated when HOST mode is changed.) |
| 3 | RESERVED | 0 | N | N | R | Reserved |
| 2 | THREG_STAT | 0 | N | N | R | Thermal regulation status<br>0: Normal (Default)<br>1: In thermal regulation |
| 1 | DPDM_STAT | 0 | N | N | R | D+/D- detection status bits<br>0: The D+/D- detection is NOT started yet, or the detection is done (Default)<br>1: The D+/D- detection is ongoing |
| 0 | VBAT_PG_STAT | 0 | N | N | R | VBAT power good status<br>0: VBAT NOT power good (Default)<br>1: VBAT power good<br>(Notice: VBAT > VBAT_UVLO) |

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Register Address: 0x1E, Register Name: CHG_STATUS 3

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | ACRB2_STAT | 0 | N | N | R | The ACFET2-RBFET2 status<br>0: ACFET2-RBFET2 is NOT placed (Default)<br>1: ACFET2-RBFET2 is placed |
| 6 | ACRB1_STAT | 0 | N | N | R | The ACFET1-RBFET1 status<br>0: ACFET1-RBFET1 is NOT placed (Default)<br>1: ACFET1-RBFET1 is placed |
| 5 | ADC_DONE_STAT | 0 | N | N | R | ADC status (in one-shot mode only)<br>0: ADC NOT complete (Default)<br>1: ADC done |
| 4 | VSYSMIN_STAT | 0 | N | N | R | VSYS_MIN Regulation Status<br>0: Not in SYS_MIN regulation (VBAT > VSYS_MIN) (Default)<br>1: In SYS_MIN regulation (VBAT < VSYS_MIN) |
| 3 | FASTCHG_TMR_STAT | 0 | N | N | R | Fast charge safety timer status<br>0: Normal (Default)<br>1: Fast charge safety timer timeout |
| 2 | TRICHG_TMR_STAT | 0 | N | N | R | Trickle charge safety timer status<br>0: Normal (Default)<br>1: Trickle charge safety timer timeout |
| 1 | PRECHG_TMR_STAT | 0 | N | N | R | Pre-charge safety timer status<br>0: Normal (Default)<br>1: Pre-charge safety timer timeout |
| 0 | RESERVED | 0 | N | N | R | Reserved |

Register Address: 0x1F, Register Name: CHG_STATUS 4

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:4 | RESERVED | 0000 | N | N | R | Reserved |
| 3 | JEITA_COLD_STAT | 0 | N | N | R | The TS temperature is in the cold range<br>0: NOT in cold range (Default)<br>1: In cold range |
| 2 | JEITA_COOL_STAT | 0 | N | N | R | The TS temperature is in the cool range<br>0: NOT in cool range (Default)<br>1: In cool range |
| 1 | JEITA_WARM_STAT | 0 | N | N | R | The TS temperature is in the warm range<br>0: NOT in warm range (Default)<br>1: In warm range |
| 0 | JEITA_HOT_STAT | 0 | N | N | R | The TS temperature is in the hot range<br>0: NOT in hot range (Default)<br>1: In hot range |

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Register Address: 0x20, Register Name: FAULT_STATUS 0

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | IBAT_REG_STAT | 0 | N | N | R | IBAT regulation when in OTG mode<br>0: Not in battery current regulation (Default)<br>1: In battery current regulation |
| 6 | VBUS_OVP_STAT | 0 | N | N | R | VBUS overvoltage protection status<br>0: Not in VBUS OVP (Default)<br>1: In VBUS OVP |
| 5 | VBAT_OVP_STAT | 0 | N | N | R | VBAT overvoltage protection status<br>0: Not in VBAT OVP (Default)<br>1: In VBAT OVP |
| 4:3 | RESERVED | 00 | N | N | R | Reserved |
| 2 | CYC_OCP_STAT | 0 | N | N | R | Converter cycle-by-cycle overcurrent protection status<br>0: Not in Cycle-by-Cycle OCP (Default)<br>1: In Cycle-by-Cycle OCP |
| 1 | VAC2_OVP_STAT | 0 | N | N | R | VAC2 overvoltage protection status<br>0: Not in VAC2 OVP (Default)<br>1: In VAC2 OVP |
| 0 | VAC1_OVP_STAT | 0 | N | N | R | VAC1 overvoltage protection status<br>0: Not in VAC1 OVP (Default)<br>1: In VAC1 OVP |

Register Address: 0x21, Register Name: FAULT_STATUS 1

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | VSYS_UVP_STAT | 0 | N | N | R | VSYS undervoltage protection status<br>0: Not in VSYS UVP (Default)<br>1: In VSYS UVP |
| 6 | VSYS_OVP_STAT | 0 | N | N | R | VSYS overvoltage protection status<br>0: Not in VSYS OVP (Default)<br>1: In VSYS OVP |
| 5 | OTG_OVP_STAT | 0 | N | N | R | OTG overvoltage protection status<br>0: Not in OTG OVP (Default)<br>1: In OTG OVP |
| 4:3 | RESERVED | 00 | N | N | R | Reserved |
| 2 | TOTP_STAT | 0 | N | N | R | IC over-temperature shutdown status<br>0: Not in OTP (Default)<br>1: In OTP |
| 1:0 | RESERVED | 00 | N | N | R | Reserved |

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Register Address: 0x22, Register Name: CHG_IRQ_FLAG 0

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | AICR_FLAG | 0 | N | N | R | AICR flag or OTG_CC flag<br>0: Normal (Default)<br>1: Any change in AICR_STAT/OTG_CC_STAT, read clear |
| 6 | MIVR_FLAG | 0 | N | N | R | MIVR flag or OTG_CV flag<br>0: Normal (Default)<br>1: Any change in MIVR_STAT/OTG_CV_STAT, read clear |
| 5 | WDT_FLAG | 0 | N | N | R | $I^2C$ watchdog timer flag<br>0: Normal (Default)<br>1: WDT_STAT rising, read clear |
| 4 | BAD_ADAPTER_FLAG | 0 | N | N | R | Bad adapter detection flag<br>0: Normal (Default)<br>1: BAD_ADAPTER_STAT rising, read clear |
| 3 | VBUS_GD_RDY_FLAG | 0 | N | N | R | VBUS good ready for charge flag<br>0: Normal (Default)<br>1: Any change in VBUS_GD_RDY_STAT even, read clear |
| 2 | VAC2_PG_FLAG | 0 | N | N | R | VAC2 power good flag<br>0: Normal (Default)<br>1: Any change in VAC2_PG_STAT, read clear |
| 1 | VAC1_PG_FLAG | 0 | N | N | R | VAC1 power good flag<br>0: Normal (Default)<br>1: Any change in VAC1_PG_STAT, read clear |
| 0 | VBUS_PG_FLAG | 0 | N | N | R | VBUS power good flag<br>0: Normal (Default)<br>1: Any change in VBUS_PG_STAT, read clear |

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Register Address: 0x23 Register Name: CHG_IRQ_FLAG 1

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | CHG_FLAG | 0 | N | N | R | Charge status flag<br>0: Normal (Default)<br>1: Any change in CHG_STAT, read clear |
| 6 | AICC_FLAG | 0 | N | N | R | AICC status flag<br>0: Normal (Default)<br>1:Any change in AICC_STAT, read clear |
| 5 | RESERVED | 0 | N | N | R | Reserved |
| 4 | VBUS_FLAG | 0 | N | N | R | VBUS status flag<br>0: Normal (Default)<br>1: Any change in VBUS_STAT, read clear |
| 3 | RESERVED | 0 | N | N | R | Reserved |
| 2 | THREG_FLAG | 0 | N | N | R | IC thermal regulation flag<br>0: Normal (Default)<br>1: THREG_STAT rising, read clear |
| 1 | VBAT_PG_ FLAG | 0 | N | N | R | VBAT power good flag<br>0: Normal (Default)<br>1: Any change in VBAT_PG_STAT, read clear |
| 0 | BC1.2_ DONE_FLAG | 0 | N | N | R | BC1.2 done Flag<br>0: BC1.2 detection not ready (Default)<br>1: BC12_DONE_STAT rising detection done, read clear |

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Register Address: 0x24 Register Name: CHG_IRQ_FLAG 2

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | RESERVED | 0 | N | N | R | Reserved |
| 6 | DPDM_DONE_FLAG | 0 | N | N | R | D+/D- detection is done flag.<br>0: D+/D- detection is NOT started or still ongoing (Default)<br>1: D+/D- detection is completed, read clear |
| 5 | ADC_DONE_FLAG | 0 | N | N | R | ADC done flag (only in one-shot mode)<br>0: ADC NOT completed (Default)<br>1: ADC done, read clear |
| 4 | VSYSMIN_FLAG | 0 | N | N | R | VSYSMIN regulation flag<br>0: Normal (Default)<br>1: Any change in VSYSMIN_STAT, read clear |
| 3 | FASTCHG_TMR_FLAG | 0 | N | N | R | Fast charge timer timeout flag<br>0: Normal (Default)<br>1: FASTCHG_TMR_STAT rising, read clear |
| 2 | TRICHG_TMR_FLAG | 0 | N | N | R | Trickle charge timer timeout flag<br>0: Normal (Default)<br>1: TRICHG_TMR_STAT rising, read clear |
| 1 | PRECHG_TMR_FLAG | 0 | N | N | R | Pre-charge timer timeout flag<br>0: Normal (Default)<br>1: PRECHG_TMR_STAT rising, read clear |
| 0 | BG_TMR_FLAG | 0 | N | N | R | Back-ground charge timer flag<br>0: Normal (Default)<br>1: Back-ground charge timer timeout rising, read clear |

Register Address: 0x25 Register Name: CHG_IRQ_FLAG 3

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:5 | RESERVED | 000 | N | N | R | Reserved |
| 4 | OTG_LBP_FLAG | 0 | N | N | R | The VBAT is under OTG_LBP<br>0: Normal (Default)<br>1: OTG_LBP_STAT rising, read clear |
| 3 | JEITA_COLD_FLAG | 0 | N | N | R | JEITA_COLD flag<br>0: Normal (Default)<br>1: JEITA_COLD_STAT rising, read clear |
| 2 | JEITA_COOL_FLAG | 0 | N | N | R | JEITA_COOL flag<br>0: Normal (Default)<br>1: JEITA_COOL_STAT rising, read clear |
| 1 | JEITA_WARM_FLAG | 0 | N | N | R | JEITA_COOL flag<br>0: Normal (Default)<br>1: JEITA_WARM_STAT rising, read clear |
| 0 | JEITA_HOT_FLAG | 0 | N | N | R | JEITA_HOT flag<br>0: Normal (Default)<br>1: JEITA_HOT_STAT rising, read clear |

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Register Address: 0x26 Register Name: CHG_IRQ_FLAG 4

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | IBAT_REG_FLAG | 0 | N | N | R | When in OTG, IBAT regulation flag<br>0: Normal (Default)<br>1: Any change in IBAT_STAT, read clear |
| 6 | VBUS_OVP_FLAG | 0 | N | N | R | VBUS overvoltage protection flag<br>0: Normal (Default)<br>1: VBUS_OVP_STAT rising, read clear |
| 5 | VBAT_OVP_FLAG | 0 | N | N | R | VBAT overvoltage protection flag<br>0: Normal (Default)<br>1: VBAT_OVP_STAT rising, read clear |
| 4 | IBUS_OCP_FLAG | 0 | N | N | R | IBUS overcurrent protection flag<br>0: Normal (Default)<br>1: IBUS_OCP_STAT rising, read clear |
| 3 | IBAT_OCP_FLAG | 0 | N | N | R | IBAT overcurrent protection flag<br>0: Normal (Default)<br>1: IBAT_OCP_STAT rising, read clear |
| 2 | CYC_OCP_FLAG | 0 | N | N | R | Cycle-by-cycle overcurrent protection flag<br>0: Normal (Default)<br>1: CYC_OCP_FLAG rising, read clear |
| 1 | VAC2_OVP_FLAG | 0 | N | N | R | VAC2 overvoltage protection flag<br>0: Normal (Default)<br>1: VAC2_OVP_STAT rising, read clear |
| 0 | VAC1_OVP_FLAG | 0 | N | N | R | VAC1 overvoltage protection flag<br>0: Normal (Default)<br>1: VAC1_OVP_STAT rising, read clear |

Register Address: 0x27 Register Name: CHG_IRQ_FLAG 5

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | VSYS_UVP_FLAG | 0 | N | N | R | VSYS undervoltage protection flag<br>0: Normal (Default)<br>1: VSYS_UVP_STAT rising, read clear |
| 6 | VSYS_OVP_FLAG | 0 | N | N | R | VSYS overvoltage flag<br>0: Normal (Default)<br>1: VSYS_OVP_STAT rising, read clear |
| 5 | OTG_OVP_FLAG | 0 | N | N | R | OTG overvoltage flag<br>0: Normal (Default)<br>1: OTG_OVP_STAT rising, read clear |
| 4 | OTG_UVP_FLAG | 0 | N | N | R | OTG undervoltage flag<br>0: Normal (Default)<br>1: OTG_UVP_STAT rising, read clear |
| 3 | RESERVED | 0 | N | N | R | Reserved |
| 2 | TOTP_FLAG | 0 | N | N | R | IC thermal shutdown flag<br>0: Normal (Default)<br>1: TOTP_STAT rising, read clear |
| 1:0 | RESERVED | 00 | N | N | R | Reserved |

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Register Address: 0x28 Register Name: CHG_IRQ_MASK 0

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | AICR_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of AICR_FLAG (Default)<br>1: Mask IRQ of AICR_FLAG |
| 6 | MIVR_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of MIVR_FLAG (Default)<br>1: Mask IRQ of MIVR_FLAG |
| 5 | WDT_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of WDT_FLAG (Default)<br>1: Mask IRQ of WDT_FLAG |
| 4 | BAD_ADAPTER_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of BAD_ADAPTER_FLAG (Default)<br>1: Mask IRQ of BAD_ADAPTER_FLAG |
| 3 | VBUS_GD_RDY _MASK | 0 | N | Y | R/W | 0: Not mask IRQ of VBUS_GD_RDY_FLAG (Default)<br>1: Mask IRQ of VBUS_GD_RDY_FLAG |
| 2 | VAC2_PG_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of VAC2_PG_FLAG (Default)<br>1: Mask IRQ of VAC2_PG_FLAG |
| 1 | VAC1_PG_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of VAC1_PG_FLAG (Default)<br>1: Mask IRQ of VAC1_PG_FLAG |
| 0 | VBUS_PG_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of VBUS_PG_FLAG (Default)<br>1: Mask IRQ of VBUS_PG_FLAG |

Register Address: 0x29 Register Name: CHG_IRQ_MASK 1

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | CHG_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of CHG_FLAG (Default)<br>1: Mask IRQ of CHG_FLAG |
| 6 | AICC_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of AICC_FLAG (Default)<br>1: Mask IRQ of AICC_FLAG |
| 5 | RESERVED | 0 | N | N | R | Reserved |
| 4 | VBUS_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of VBUS_FLAG (Default)<br>1: Mask IRQ of VBUS_FLAG |
| 3 | RESERVED | 0 | N | N | R | Reserved |
| 2 | THREG_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of THREG_FLAG (Default)<br>1: Mask IRQ of THREG_FLAG |
| 1 | VBAT_PG_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of VBAT_PG_FLAG (Default)<br>1: Mask IRQ of VBAT_PG_FLAG |
| 0 | BC1.2_DONE_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of BC1.2_DONE_FLAG (Default)<br>1: Mask IRQ of BC1.2_DONE_FLAG |

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Register Address: 0x2A Register Name: CHG_IRQ_MASK 2

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | RESERVED | 0 | N | N | R | Reserved |
| 6 | DPDM_DONE _MASK | 0 | N | Y | R/W | 0: Not mask IRQ of DPDM_DONE_FLAG (Default)<br>1: Mask IRQ of DPDM_DONE_FLAG |
| 5 | ADC_DONE_ MASK | 0 | N | Y | R/W | 0: Not mask IRQ of ADC_DONE (Default)<br>1: Mask IRQ of ADC_DONEG |
| 4 | VSYSMIN_ MASK | 0 | N | Y | R/W | 0: Not mask IRQ of VSYSMIN_FLAG (Default)<br>1: Mask IRQ of VSYSMIN_FLAG |
| 3 | FASTCHG_ TMR_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of FASTCHG_TMR_FLAG (Default)<br>1: Mask IRQ of FASTCHG_TMR_FLAG |
| 2 | TRICHG_TMR _MASK | 0 | N | Y | R/W | 0: Not mask IRQ of TRICHG_TMR_FLAG (Default)<br>1: Mask IRQ of TRICHG_TMR_FLAG |
| 1 | PRECHG_ TMR_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of PRECHG_TMR_FLAG (Default)<br>1: Mask IRQ of PRECHG_TMR_FLAG |
| 0 | BG_TMR_ MASK | 0 | N | Y | R/W | 0: Not mask IRQ of BG_TMR_FLAG (Default)<br>1: Mask IRQ of BG_TMR_FLAG |

Register Address: 0x2B Register Name: CHG_IRQ_MASK 3

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:5 | RESERVED | 000 | N | N | R | Reserved |
| 4 | OTG_LBP_ MASK | 0 | Y | Y | R/W | 0: Not mask IRQ of OTG_LBP_FLAG (Default)<br>1: Mask IRQ of OTG_LBP_FLAG |
| 3 | JEITA_COLD_ MASK | 0 | Y | Y | R/W | 0: Not mask IRQ of JEITA_COLD_FLAG (Default)<br>1: Mask IRQ of JEITA_COLD_FLAG |
| 2 | JEITA_COOL_ MASK | 0 | Y | Y | R/W | 0: Not mask IRQ of JEITA_COOL_FLAG (Default)<br>1: Mask IRQ of JEITA_COOL_FLAG |
| 1 | JEITA_WARM _MASK | 0 | Y | Y | R/W | 0: Not mask IRQ of JEITA_WARM_FLAG (Default)<br>1: Mask IRQ of JEITA_WARM_FLAG |
| 0 | JEITA_HOT_ MASK | 0 | Y | Y | R/W | 0: Not mask IRQ of JEITA_HOT_FLAG (Default)<br>1: Mask IRQ of JEITA_HOT_FLAG |

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Register Address: 0x2C Register Name: CHG_IRQ_MASK 4

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | IBAT_REG_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of IBAT_REG_FLAG (Default)<br>1: Mask IRQ of IBAT_REG_FLAG |
| 6 | VBUS_OVP_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of VBUS_OVP_FLAG (Default)<br>1: Mask IRQ of VBUS_OVP_FLAG |
| 5 | VBAT_OVP_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of VBAT_OVP_FLAG (Default)<br>1: Mask IRQ of VBAT_OVP_FLAG |
| 4 | IBUS_OCP_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of IBUS_OCP_FLAG (Default)<br>1: Mask IRQ of IBUS_OCP_FLAG |
| 3 | IBAT_OCP_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of IBAT_OCP_FLAG (Default)<br>1: Mask IRQ of IBAT_OCP_FLAG |
| 2 | CYC_OCP_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of CYC_OCP_FLAG (Default)<br>1: Mask IRQ of CYC_OCP_FLAG |
| 1 | VAC2_OVP_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of VAC2_OVP_FLAG (Default)<br>1: Mask IRQ of VAC2_OVP_FLAG |
| 0 | VAC1_OVP_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of VAC1_OVP_FLAG (Default)<br>1: Mask IRQ of VAC1_OVP_FLAG |

Register Address: 0x2D Register Name: CHG_IRQ_MASK 5

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | VSYS_UVP_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of VSYS_UVP_FLAG (Default)<br>1: Mask IRQ of VSYS_UVP_FLAG |
| 6 | VSYS_OVP_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of VSYS_OVP_FLAG (Default)<br>1: Mask IRQ of VSYS_OVP_FLAG |
| 5 | OTG_OVP_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of OTG_OVP_FLAG (Default)<br>1: Mask IRQ of OTG_OVP_FLAG |
| 4 | OTG_UVP_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of OTG_UVP_FLAG (Default)<br>1: Mask IRQ of OTG_UVP_FLAG |
| 3 | RESERVED | 0 | N | N | R | Reserved |
| 2 | TOTP_MASK | 0 | N | Y | R/W | 0: Not mask IRQ of TOTP_FLAG (Default)<br>1: Mask IRQ of TOTP_FLAG |
| 1:0 | RESERVED | 00 | N | N | R | Reserved |

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Register Address: 0x2E Register Name: ADC_CTRL

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | ADC_EN | 0 | Y | Y | R/W | ADC control<br>0: Disable (Default)<br>1: Enable<br>(Back to 0, when one shot conversion finish.) |
| 6 | ADC_CONV_CTRL | 0 | N | Y | R/W | ADC conversion control<br>0: Continuous conversion (Default)<br>1: One shot conversion |
| 5:0 | RESERVED | 000000 | N | N | R | Reserved |

Register Address: 0x2F Register Name: ADC_CNANNEL 0

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | IBUS_ADC_DIS | 0 | N | Y | R/W | IBUS ADC control<br>0: Enable (Default)<br>1: Disable |
| 6 | IBAT_ADC_DIS | 0 | N | Y | R/W | IBAT ADC control<br>0: Enable (Default)<br>1: Disable |
| 5 | VBUS_ADC_DIS | 0 | N | Y | R/W | VBUS ADC control<br>0: Enable (Default)<br>1: Disable |
| 4 | VBAT_ADC_DIS | 0 | N | Y | R/W | VBAT ADC control<br>0: Enable (Default)<br>1: Disable |
| 3 | VSYS_ADC_DIS | 0 | N | Y | R/W | VSYS ADC control<br>0: Enable (Default)<br>1: Disable |
| 2 | TS_ADC_DIS | 0 | N | Y | R/W | TS ADC control<br>0: Enable (Default)<br>1: Disable |
| 1 | TDIE_ADC_DIS | 0 | N | Y | R/W | TDIE ADC control<br>0: Enable (Default)<br>1: Disable |
| 0 | RESERVED | 1 | Y | Y | R/W | Reserved |

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Register Address: 0x30 Register Name: ADC_CNANNEL 1

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | DP_ADC_DIS | 0 | N | Y | R/W | D+ ADC control<br>0: Enable (Default)<br>1: Disable |
| 6 | DM_ADC_DIS | 0 | N | Y | R/W | D- ADC control<br>0: Enable (Default)<br>1: Disable |
| 5 | VAC2_ADC_DIS | 0 | N | Y | R/W | VAC2 ADC control<br>0: Enable (Default)<br>1: Disable |
| 4 | VAC1_ADC_DIS | 0 | N | Y | R/W | VAC1 ADC control<br>0: Enable (Default)<br>1: Disable |
| 3:0 | RESERVED | 0000 | N | N | R | Reserved |

Register Address: 0x31 Register Name: IBUS_ADC

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:0 | IBUS_ADC | 0 | N | N | R | IBUS ADC reading, LSB: 1mA<br>Reported in 2's complement for discharge value.<br>IBUS ADC reports charge value and discharge value.<br>(Notice: Charge: VBUS to PMID; Discharge: PMID to VBUS) |

Register Address: 0x33 Register Name: IBAT_ADC

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:0 | IBAT_ADC | 0 | N | N | R | IBAT ADC reading, LSB: 1mA<br>Reported in 2's complement for discharge value.<br>IBAT ADC reports charge value and discharge value.<br>(Notice: Charge: VSYS to VBAT; Discharge: VBAT to VSYS) |

Register Address: 0x35 Register Name: VBUS_ADC

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:0 | VBUS_ADC | 0 | N | N | R | VBUS ADC reading, LSB: 1mV |

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Register Address: 0x37 Register Name: VAC1_ADC

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:0 | VAC1_ADC | 0 | N | N | R | VAC1 ADC reading, LSB: 1mV |

Register Address: 0x39 Register Name: VAC2_ADC

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:0 | VAC2_ADC | 0 | N | N | R | VAC2 ADC reading, LSB: 1mV |

Register Address: 0x3B Register Name: VBAT_ADC

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:0 | VBAT_ADC | 0 | N | N | R | VBAT ADC reading, LSB: 1mV |

Register Address: 0x3D Register Name: VSYS_ADC

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:0 | VSYS_ADC | 0 | N | N | R | VSYS ADC reading, LSB: 1mV |

Register Address: 0x3F Register Name: TS_ADC

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:0 | TS_ADC | 0 | N | N | R | TS ADC reading. LSB: 0.0963% |

Register Address: 0x41 Register Name: TDIE_ADC

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:0 | TDIE_ADC | 0 | N | N | R | TDIE ADC reading, LSB: 1°C<br>Reported in 2's complement for negative value. |

Register Address: 0x43 Register Name: DP_ADC

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:0 | DP_ADC | 0 | N | N | R | D+ ADC reading, LSB: 1mV |

Register Address: 0x45 Register Name: DM_ADC

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 15:0 | DM_ADC | 0 | N | N | R | D- ADC reading, LSB: 1mV |

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Register Address: 0x47 Register Name: DPDM_MANU_CTRL

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:5 | DP_CTRL | 000 | N | N | R/W | D+ manual control<br>000: HIZ (Default)<br>001: 0<br>010: 0.6V<br>011: 1.2V<br>100: 2.0V<br>101: 2.7V<br>110: 3.3V<br>111: Reserved |
| 4:2 | DM_CTRL | 000 | N | N | R/W | D- manual control<br>000: HIZ (Default)<br>001: 0<br>010: 0.6V<br>011: 1.2V<br>100: 2.0V<br>101: 2.7V<br>110: 3.3V<br>111: Reserved |
| 1:0 | RESERVED | 00 | N | N | R | Reserved |

Register Address: 0x48 Register Name: DEVICE_INFO

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | RESERVED | 0 | N | N | R | Reserved |
| 6:3 | DEVICE_ID | 1110 | N | N | R | 1110: RT9492 |
| 2:0 | RESERVED | 000 | N | N | R | Reserved |

Register Address: 0x49 Register Name: PUMP_EXP

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | PE_EN | 0 | Y | Y | RWSC | 0: Disable (Default)<br>1: MTK Pump Express process enable<br>(Back to 0 while PE done or no VBUS) |
| 6 | PE_SEL | 0 | Y | Y | R/W | 0: PE 1.0 process select (Default)<br>1: PE 2.0 process select |
| 5 | PE10_INC | 0 | Y | Y | R/W | 0: PE 1.0 Voltage down (Default)<br>1: PE 1.0 Voltage up |
| 4:0 | PE20_CODE | 00000 | Y | Y | R/W | MTK PE 2.0 voltage request setting<br>00000: 5.5V (Default)<br>00001: 6V<br>…<br>11101: 20V<br>11110: Adapter healthy self-testing<br>11111: Disable cable drop compensation |

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Register Address: 0x4A Register Name: ADD_CTRL 0

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | DIS_I2C_TO | 0 | Y | Y | R/W | Reset $I^2C$ slave after RT9492 latch SDA low for 1s<br>0: Enable $I^2C$ time-out function (Default)<br>1: Disable $I^2C$ time-out function |
| 6 | QON_RST_EN | 1 | Y | Y | R/W | 0: QON pin = 0 for 10s will NOT do any thing<br>1: QON pin = 0 for 10s will turn off Ship FET and stop switching to reset system power (Default) |
| 5 | AUTO_AICR | 1 | Y | Y | R/W | 0: No action<br>1: Auto set IAICR by BC1.2 done (Default) |
| 4 | TD_EOC | 1 | Y | Y | R/W | End-of-charge deglitch time<br>0: 2ms<br>1: 64ms (Default) |
| 3 | EOC_RST | 0 | Y | Y | RWC | 0: No action (Default)<br>1: Reset EOC<br>auto clear after reset EOC done |
| 2 | AUTO_MIVR | 1 | Y | Y | R/W | 0: No action<br>1: Auto set MIVR by VBUS plug-in (Default) |
| 1 | JEITA_COOL_VSET | 1 | Y | Y | R/W | 0: Set VBAT_REG = JEITA_WARM_VSET setting (REG0x17[7:5])<br>1: VBAT_REG = Register setting (Default) |
| 0 | JEITA_COLD_HOT | 0 | Y | Y | R/W | 0: JEITA_COLD or JEITA_HOT, stop charge/OTG (Default)<br>1: JEITA_COLD or JEITA_HOT, still charge/OTG |

Register Address: 0x4B Register Name: ADD_CTRL 1

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7:5 | RESERVED | 000 | N | N | R | Reserved |
| 4 | PWM_1MHZ_EN | 0 | N | Y | R/W | Enable PWM frequency 1MHz mode<br>0: PWM frequency follow PWM_FREQ (Default)<br>1: Enable PWM frequency at 1MHz |
| 3 | OTG_PIN_EN | 0 | Y | Y | R/W | 0: OTG pin function disable (Default)<br>1: OTG pin function enable |
| 2 | OTG_EN_CONTROL | 0 | Y | Y | R/W | OTG mode enable with OTG pin<br>0: Enable OTG mode by OTG_EN bit (Default)<br>1: Enable OTG by both OTG_EN bit and OTG pin |
| 1:0 | SEAMLESS_CONTROL | 00 | Y | Y | R/W | 00: Disable (Default)<br>01: Seamless on VBUS<br>10: Seamless on VAC1<br>11: Seamless on VAC2 |

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Register Address: 0x4C Register Name: ADD_CTRL 2

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | BC12_EN_CHANNEL | 0 | Y | Y | R/W | BC12 detect channel<br>0: VAC1 (Default)<br>1: VAC2 |
| 6:5 | DCDT_SEL | 10 | Y | Y | R/W | BC1.2 Data contact timer<br>00: Disable DCD timeout function<br>01: Enable 300ms DCD timeout function<br>10: Enable 600ms DCD timeout function (Default)<br>11: Wait data contact |
| 4 | VLGC_OPT | 0 | Y | Y | R/W | Enable primary detection high reference voltage option<br>0: Disable (Default)<br>1: Enable |
| 3 | DPDM_CMP_HYS_EN | 1 | Y | Y | R/W | DPDM detection hysteresis enable control<br>0: Disable<br>1: Enable (Default) |
| 2 | SPEC_TA_EN | 1 | Y | Y | R/W | 0: Disable Special TA detection<br>1: Enable Special TA detection (Default) |
| 1:0 | HOST_MODE | 00 | Y | Y | R/W | Host mode setting in OTG<br>00: DPDM floating (Default)<br>01: SDP<br>10: CDP<br>11: DCP |

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Register Address: 0x4D Register Name: CHG_IRQ_FLAG 6

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | IEOC_FLAG | 0 | N | N | R | IEOC flag<br>0: Not trigger IEOC (Default)<br>1: Trigger IEOC STAT, read clear |
| 6 | VSYS_ SHORT_FLAG | 0 | N | N | R | Short Circuit Protect between VSYS-VBAT flag<br>0: Not trigger VSYS_SHORT (Default)<br>1: Trigger VSYS_SHORT, read clear |
| 5 | REGN_PROT ECT_FLAG | 0 | N | N | R | REGN overcurrent or undervoltage protection flag<br>0: Not trigger REGN_PROTECT (Default)<br>1: Trigger REGN_PROTECT, read clear |
| 4 | PE_DONE_ FLAG | 0 | N | N | R | Pump Express process flag<br>0: PE_DONE_FLAG not rising (Default)<br>1: While PE processing done, read clear |
| 3 | VBUS_ UNDER_MIVR _FLAG | 0 | N | N | R | VBUS falling under MIVR flag<br>0: VBUS not falling under MIVR (Default)<br>1: VBUS falling under MIVR, read clear |
| 2 | VRECHG_ FLAG | 0 | N | N | R | Recharger event flag<br>0: No event happened (Default)<br>1: VBAT < VRECHG after EOC, read clear |
| 1 | CDP_PD_ FLAG | 0 | N | N | R | CDP primary detection start<br>0: CDP primary detection does not start (Default)<br>1: CDP primary detection starts, read clear |
| 0 | CDP_DONE_ FLAG | 0 | N | N | R | CDP flow done<br>0: No CDP flow (Default)<br>1: CDP flow done, read clear |

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Register Address: 0x4E Register Name: CHG_IRQ_MASK 6

| Bit | Bit Name | Default | WDT RST | REG RST | Type | Description |
|---|---|---|---|---|---|---|
| 7 | IEOC_MASK | 1 | Y | Y | R/W | 0: Not mask IRQ of IEOC_FLAG<br>1: Mask IRQ of IEOC_FLAG (Default) |
| 6 | VSYS_ SHORT_ MASK | 1 | Y | Y | R/W | 0: Not mask IRQ of VSYS_SHORT_FLAG<br>1: Mask IRQ of VSYS_SHORT_FLAG (Default) |
| 5 | REGN_ PROTECT_ MASK | 1 | Y | Y | R/W | 0: Not mask IRQ of REGN_PROTECT_FLAG<br>1: Mask IRQ of REGN_PROTECT_FLAG (Default) |
| 4 | PE_DONE_ MASK | 1 | Y | Y | R/W | 0: Not mask IRQ of PE_DONE_FLAG<br>1: Mask IRQ of PE_DONE_FLAG (Default) |
| 3 | VBUS_ UNDER_MIVR _MASK | 1 | Y | Y | R/W | 0: Not mask IRQ of VBUS_UNDER_MIVR_FLAG<br>1: Mask IRQ of VBUS_UNDER_MIVR_FLAG (Default) |
| 2 | VRECHG_ MASK | 1 | Y | Y | R/W | 0: Not mask IRQ of VRECHG_FLAG<br>1: Mask IRQ of VRECHG_FLAG (Default) |
| 1 | CDP_PD_ MASK | 1 | Y | Y | R/W | 0: Not mask IRQ of CDP_PD_FLAG<br>1: Mask IRQ of CDP_PD_FLAG (Default) |
| 0 | CDP_DONE_ MASK | 1 | Y | Y | R/W | 0: Not mask IRQ of CDP_DONE_FLAG<br>1: Mask IRQ of CDP_DONE_FLAG (Default) |

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## Application Information

(Note 9)

### Power-On-Reset (POR)

The device powers internal bias circuits from the higher voltage of VAC1/ VAC2, VBUS, VBATP and VBAT. When VAC1/ VAC2 rises above $V_{AC_UVLO}$, VBUS rises above $V_{BUS_UVLO}$, VBATP rises above $V_{BATP_UVLO}$ or VBAT rises above $V_{BAT_UVLO}$, $I^2C$ interface is ready for communication and all the registers are reset to default value.

- **PROG Pin for Cell and Frequency Setting**

  During POR stage, the device detects the PROG pin pull-down resistance, and then sets register 0x0A[7:6] for BATTERY_CELL and register 0x13[5] for PWM_FREQ. Please follow Table 1 for PROG pin pull-down resistor selection. The pull-down resistor on the PROG pin is recommended to have ±1% to 2% tolerance for its resistance.

- **BATTERY_CELL for Default Charging Parameter**

  After the PROG pin detected, the BATTERY_CELL will set by PROG pull-down resistance, and then the following registers in Table 2 will be set by BATTERY_CELL for default charging parameters.

**Table 1. PROG Pin Resistance for Cell and Frequency Setting**

| Cell | Resistance for Typical Value | Frequency | BATTERY_CELL | PWM_FREQ |
|---|---|---|---|---|
| 2s | 6.04kΩ | 1.5MHz | 01 | 0 |
| | 8.2kΩ | 750kHz | | 1 |
| 3s | 10.5kΩ | 1.5MHz | 10 | 0 |
| | 13.7kΩ | 750kHz | | 1 |
| 4s | 17.4kΩ | 1.5MHz | 11 | 0 |
| | 27.0kΩ | 750kHz | | 1 |

**Table 2. Default Register Setting for Charging Parameter by BATTERY_CELL**

| BATTERY_CELL (REG0x0A[7:6]) | 2s | 3s | 4s |
|---|---|---|---|
| VSYSMIN (REG 0x00[5:0]) | 7V | 9V | 12V |
| VBAT_REG (REG 0x01[10:0]) | 8.4V | 12.6V | 16.8V |
| VBAT_REG range | 5V to 9.99V | 10V to 13.99V | 14V to 18.8V |
| ICHG_CTRL (REG 0x03[8:0]) | 2A | 1A | 1A |

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After POR, the charging parameters shown in Table 2 can be programmed by $I^2C$; however, the VBAT_REG has programming range regarding BATTERY_CELL setting, so the host needs to ensure the program value within the right range. If the host programs the value out of the range, the charger will ignore and keeps at the original value. The charging parameters in Table 2 can be changed by programming BATTERY_CELL. When the host needs to program any parameter in REG0x0A, the host must program REG0x0A at first, then the host can program other registers.

- **Device Power Up from Battery Only**

  When only Battery is present and VBATP above $V_{BATP_UVLO}$, the SHIPFET turns on to connect VBATP to VBAT. Then, when VBAT above $V_{BAT_UVLO}$, the BATFET turns on to connect VBAT to VSYS. The REGN stays off to minimize the quiescent current. The low quiescent current on VBAT and low $R_{DS(ON)}$ of BATFET minimizes device power consumption and conduction loss, which maximize battery run life.

  The device always monitors the discharge current through BATFET (Battery Supply Mode). When the system is shorted or overloaded ($I_{BAT} > I_{BAT_OCP}$), if SHIP_FET_PRESENT = 1 (0x14, bit[7]) and EN_BATOC = 1 (0x14, bit[0]), the device turns off SHIPFET and BATFET immediately to enter Shipping Mode until VBUS is plugged in again or uses the methods to Exit Shipping Mode to re-enable BATFET.

### Dual-Input Power Selection

The charger has two ACDRV drivers to control optional back-to-back N-channel MOSFET for input power source selection. During POR, ACDRV pin detects whether optional AC-RBFET is present or not, then updates status to ACRB1_STAT and ACRB2_STAT. Table 3 shows the detailed status.

**Table 3. Optional AC-RBFET Status for Input Power Selection**

| Scenario | AC-RBFET 1 present | AC-RBFET 2 present | ACDRV1 pin | ACDRV2 pin | ACRB1_STAT | ACRB2_STAT |
|---|---|---|---|---|---|---|
| Single Input | N | N | GND | GND | 0 | 0 |
| One AC-RBFET | Y | N | Gate | GND | 1 | 0 |
| | N | Y | GND | Gate | 0 | 1 |
| Dual Input | Y | Y | Gate | Gate | 1 | 1 |

- **Single Input**

  In this scenario, input power source comes only from VBUS, both of VAC1 and VAC2 connect to VBUS. After POR, control register EN_ACDRV1 and EN_ACDRV2 keep at 0.

- **One AC-RBFET**

  In this scenario, only AC-RBFET1 or AC-RBFET2 is present; for example, only AC-RBFET1 is present, the ACDRV1 connects to AC-RBFET1 gate, and the ACDRV2 pulls down to GND. VAC2 connects to VBUS. After POR, register EN_ACDRV2 keeps at 0.

  1. When $V_{AC1} > V_{AC_UVLO}$, the charger forces register EN_ACDRV1 = 1 to turn on AC-RBFET1.
  2. To swap input source from VAC1 to another power source, at first, the host has to set register DIS_ACDRV_EN = 1 to force EN_ACDRV1 = 0 to turn off AC-RBFET1; after $V_{BUS} < V_{BUS_UVLO}$, the host enables another power source to directly connect to VBUS for input power source.

- **Dual Input**

  In this scenario, both of AC-RBFET1 and AC-RBFET2 are present.

  1. VAC1 is plugged in, when $V_{AC1} > V_{AC_UVLO}$, the charger sets register EN_ACDRV1 = 1 to turn on AC-RBFET1.
  2. Then VAC2 is plugged in, when $V_{AC2} > V_{AC_UVLO}$, the charger still sets register EN_ACDRV1 = 1.
  3. To swap input power source from VAC1 to VAC2, the host has to set EN_ACDRV1 = 0 and

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EN_ACDRV2 = 1 at the same time, after register is programmed, charger turns off AC-RBFET1.

4. After VBUS < $V_{BUS_UVLO}$, the charger automatically turns on AC-RBFET2 to swap input power source from VAC1 to VAC2.
5. When VAC2 is plugged out, after VAC2 < $V_{AC_UVLO}$, then charger sets EN_ACDRV2 = 0 to turn off AC-RBFET2.
6. After VBUS < $V_{BUS_UVLO}$, charger automatically sets EN_ACDRV1 from 0 to 1 to turn on AC-RBFET1.
7. When VAC1 is plugged out, after VAC1 < $V_{AC_UVLO}$, the charger sets EN_ACDRV1 = 0 to turn off AC-RBFET1.

If both of VAC1 > $V_{AC_UVLO}$ and VAC2 > $V_{AC_UVLO}$, and the host sets EN_ACDRV1 = 1 and EN_ACDRV2 = 1, the charger will ignore and keep original register setting. The charger does not allow to turn on AC-RBFET1 and AC-RBFET2 at the same time.

### Device Power Up from Input Power Source

When input power is present on VBUS, after VBUS is above $V_{BUS_UVLO}$, the power up sequence is as listed:

1. Power up REGN LDO.
2. Poor Source Detection
3. VBUS_STAT detection is based on input source type to set default AICR register.
4. The device detects voltage on ILIM_HZ pin to set ILIM, the final input current limit is based on the minimum value between AICR and ILIM.
5. The device detects voltage on VBUS to set default MIVR register.
6. Buck-boost converter power-up.

### Power-Up REGN LDO

The REGN LDO supplies for internal bias circuit and the buck-boost power MOSFET gate driver. The REGN also provides bias to TS and ILIM_HZ external resistor and pull-up rail of STAT and PG. The REGN is enabled when the below conditions are valid:

1. VBUS is above VBUS_UVLO
2. The charger is in OTG mode.
3. ADC TS channel is on (ADC_EN = 1 and TS_ADC_DIS = 0)
4. DPDM manual mode is on (DP_CTRL or DM_CTRL is on)

The REGN is disabled when the below conditions are valid:

1. Only VBAT with ADC TS channel is off, DPDM manual mode is off and not in OTG mode.
2. The device in HZ mode and BC1.2 is disabled.

### Poor Source Detection

After REGN powers up, the device checks the current capability of the input source. The input source has to meet the following requirements to turn on the buck converter.

1. VBUS below VBUS_OVP_RISE.
2. VBUS above VBUS_BAD_ADP then pulling IBUS_BAD_ADP (typical = 1kΩ).

When input source passes above conditions, the VBUS_GD_RDY_STAT and the VBUS_GD_RDY_FLAG turn to high and INT pin is pulsed for interrupting the host. If VBUS_GD_RDY_STAT does not turn to high, it repeats poor source detection every 2 seconds. After 8 times failures, the device sets register EN_HZ = 1 and goes to HZ mode. The register EN_HZ can be cleared to 0 by adapter re-plug in or the host sets the EN_HZ = 0. When VBUS triggers poor source detection failure, the BAD_ADAPTER_FLAG turns to high and INT pin is pulsed for interrupting the host.

### VBUS Source Type Detection

After VBUS_GD_RDY_STAT turns to high, the device runs VBUS source type detection. After detection is completed, the BC12_DONE_STAT and BC12_DONE_FLAG turn to high and INT pin is pulsed for interrupting the host. When VBUS source type detection is completed, the following registers are changed:

1. VBUS_STAT is updated to indicate VBUS source type.
2. AICR register is changed to the result of VBUS_STAT automatically if AUTO_AICR = 1, AICR setting result is listed in Table 4.

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Table 4. AICR Setting from D+/D- Detection

| Detection | AICR Setting | VBUS_STAT |
|---|---|---|
| USB SDP | 0.5A | 0001 |
| USB CDP | 1.5A | 0010 |
| USB DCP | 3.25A | 0011 |
| NSDP | 3.25A | 0101 |
| Special Adapter | 1A/2A/2.1A/2.4A | 0110 |

The device supports standard USB BC1.2 and special adapter, detection result is listed in Table 5.

Table 5. AICR Setting from Special Adapter

| D+/D- Voltage Threshold | AICR Setting |
|---|---|
| 0.9V < D+ < 1.5V | 2A |
| 1.5V < D+ < 2.3V<br>2.3V < D- | 1A |
| D+ > 2.3V<br>D- < 2.3V | 2.1A |
| D+ > 2.3V<br>D- > 2.3V | 2.4A |

### Average Input Current Regulation (AICR)

The range of AICR is from 100mA to 3.3A with 10mA resolution. When register AUTO_AICR is set to 1, the device changes AICR automatically after VBUS source type detection, refer to Table 4 and Table 5 for detailed information. After charger automatically sets AICR, register AICR is programmable by the host.

### ILIM_HZ Detection

After Poor source detection, the charger starts to detect voltage on the ILIM_HZ pin, and calculate the ILIM by the equation: $V_{ILIM_HZ}$ = 1V + 800mΩ x ILIM. When register ILIM_HZ_EN is set to 1, the charger input current limit is set by the minimum value between AICR and ILIM. If the ILIM calculation result is less than 100mA, the charger clamps ILIM at 100mA.

When the ILIM_HZ pin is pulled lower than 0.75V, the charger stops switching and REGN stays on either in charger or OTG mode. The charger resume switching when the ILIM_HZ pin voltage rises higher than 1V.

### Minimum Input Voltage Regulation (MIVR)

The MIVR function prevents input voltage from dropping due to insufficient current provided from input power source. The VBUS voltage decreases to VMIVR setting level when the overcurrent condition of input power source occurs. The register VMIVR default setting is 3.6V; It can be programmed by the host, with the range from 3.6V to 22V with 0.1V resolution. If the register AUTO_MIVR is set to 1, after poor source detection, the charger starts to detect voltage on VBUS before the charger starts switching, the register VMIVR will be set to VBUS-0.7V when VBUS < 7V, or set to VBUS-1.4V when VBUS ≥ 7V.

During charge process, if the input voltage is changed, when the register FORCE_MIVR_DET is set to 1 by the host, the charger stops switching and detect voltage on VBUS; according to above calculation equation, the register VMIVR updates to the new value, and the charger resumes switching.

When DIS_EOC_FCCM = 0 to enable FCCM to increase EOC accuracy, the MIVR setting level must set−25% voltage difference from VBAT_REG to avoid converter from working in Buck-Boost operation mode when VBUS plug out.

### Converter Power-Up

After the Input and MIVR is set, the converter is enabled and starts switching. BATFET stays on unless charger is disabled (CHG_EN = 0 or EN_PIN is pulled high).

The device integrates a synchronous PWM controller with high-accuracy current and voltage regulation, and the switching frequency is programmed with 750kHz/ 1.5MHz by the register PWM_FREQ or PROG pin. The device supports PFM control to improve light-load efficiency, also supports OOA (Out-of-Audio) control by the register DIS_CHG_OOA to prevent converter from switching in audio frequency.

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### OTG Mode Operation

The RT9490 also supports OTG (On-The-Go) mode and enters OTG mode via register EN_OTG. The maximum output current is up to 3.32A. In OTG mode, the VBUS_STAT register bits is updated to 0111, the VBUS output voltage is 5V and output limit current is 3A by default, output voltage (VOTG), output current limit (IOTG) and input current limit (IBAT_REG) can be programmed by the host. The OTG mode operation can be enabled by following condition:

1. VBAT is above VOTG_LBP rising threshold.
2. EN_OTG is set to high.
3. Voltage at TS pin is within acceptable range ($V_{VTS_HOT_OTG}$ < VTS < $V_{VTS_COLD_OTG}$).

When above conditions are passed, refer to Table 3 for AC_RBFET configuration for below setting.

- **Single Input**

  In this scenario, there is no any AC-RBFETs, the converter starts up with 4ms delay after register EN_OTG is set to 1, then VBUS voltage rises to the VOTG setting.

- **One AC-RBFET**

  In this scenario, only AC-RBFET1 or AC-RBFET2 is present; for example, if only AC-RBFET1 is present, when register EN_OTG is set to 1.

  1. The converter starts up with 4ms delay after register EN_ACDRV1 is set to 1, then VAC1 voltage rises to the VOTG setting.
  2. If register DIS_ACDRV_EN is set to 1, the converter starts up with 4ms delay, then VBUS voltage rises to the VOTG setting.

- **Dual Input**

  In this scenario, both of AC-RBFET1 and AC-RBFET2 are present, when register EN_OTG is set to 1.

  1. The converter starts up with 4ms delay after register EN_ACDRV1 is set to 1, then VAC1 voltage rises to the VOTG setting.
  2. To swap OTG output from VAC1 to VAC2, register EN_ACRDV1 is set to 0 and EN_ACDRV2 is set to 1, the device pulls low ACDRV1 pin to turn off AC-RBFET1, and pulls up ACDRV2 pin to turn on AC-RBFET2, and then VAC2 voltage rises to VOTG setting.
  3. If register DIS_ACDRV_EN is set to 1, the device forces EN_ACDRV1 and EN_ACDRV2 at 0, the converter starts up with 4ms delay, then VBUS voltage rises to VOTG setting.

  In OTG mode, if the host sets EN_ACDRV1 = 1 and EN_ACDRV2 = 1, the device will ignore and keep original register setting. The charger does not allow to turn on AC-RBFET1 and AC-RBFET2 at the same time.

  In OTG mode, the device supports PFM control to improve light-load efficiency, also supports OOA (Out-of-Audio) control by the register DIS_OTG_OOA to prevent converter from switching in the audio frequency.

  In OTG mode, the device monitors discharge current from battery. When battery discharge current is higher than register IBAT_REG setting, the device start to decrease OTG output current to keeps the systems power at the first, if the system power still increases, when OTG output voltage falls below OTG_UVP, the converter will turn off to maintain system power.

### IBAT Regulation During OTG Mode

The range of IBAT_REG is from 3A to 5A with 1A resolution. In OTG mode, when the discharge current from battery is over IBAT_REG setting, the converter starts to decrease output voltage to regulate output power from battery. The device also supports IBAT_REG disable after converter starts switching in OTG mode. When IBAT_REG is set at 11 to disable IBAT_REG before converter starts switching in OTG mode, the IBAT_REG will be set to default setting.

### Power Path Management

The device provides automatic power path selection to supply system (VSYS) from VBUS, VBAT (battery) or both of them.

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- **SHIPFET Control**

  The device supports SDRV driver for optional SHIPFET. With optional SHIPFET, after POR, the register SHIP_FET_PRESENT must set to 1 by the host, and the SHIPFET is controlled by the register SDRV_CTRL.

- **IDLE**

  When BATP is higher than VBAT_UVLO rising threshold, the SDRV pin turns on SHIPFET and the device powers on for default register setting.

- **Shutdown Mode**

  To extend battery life when shipping or storage, the device supports extremely minimum battery leakage current with shutdown mode. When device enters Shutdown Mode, the device turns off SHIPFET, internal BATFET and circuit. The only way for device to exit shutdown mode to restore power for system is by plug-in VBUS, and all registers return to default setting when the device exits shutdown mode. When in battery only condition, the device can enter shutdown mode.

- **Ship Mode**

  When device enters ship mode, the device turns off SHIPFET and internal BATFET. The device can exit Ship Mode to restore power for system by the following method:

  1. VBUS plug in
  2. Set SDRV_CTRL to IDLE
  3. Set RST_ALL or REG_RST bit to reset all registers to default
  4. Press QON pin from high to low.

  When in battery only condition, the device can enter Ship Mode.

- **System Power Reset**

  The device supports system reset via SDRV_CTRL by the host. When entering System Power Reset, the device turns off SHIPFET and BATFET; after 600ms, the device restores power for system and SDRV_CTRL goes back to IDLE. The device can enter System Power Reset even with VBUS plug in.

  The host can set SDRV_DLY = 0 to turn off SHIPFET and BATFET immediately or set SDRV _DLY = 1 to delay 10s to turn off SHIPFET and BATFET.

- **QON Pin Operation**

  The QON pin has two functions to control SHIPFET and BATFET. The register SHIP_FET_PRESENT must set to 1 by the host to enable QON function.

  - Exit Ship Mode

    Press QON pin from high to low with deglitch time by the register QON_EXIT_SHIP_DLY setting time, the device turns on SHIPFET and BATFET to restore power for system

  - SYSTEM Reset

    With register QON_RST_EN is set to 1, press QON pin from high to low with deglitch time 10s, the device turns off SHIPFET and BATFET, after 600ms, the device turns on SHIPFET and BATFET to restore power for system.

### Battery Charging Management

The device has charge current up to 5A with 9mΩ BATFET to improve charge efficiency and decrease voltage drop during battery discharging.

- **Charging Cycle**

  When battery charging is enabled (CE pin set to low and EN_CHG = 1), the device autonomously completes a charging cycle without host controls. The device default parameters are shown in Table 2. The host can also change charging parameters through $I^2C$.

  A charging cycle starts with the following condition:

  1. Buck-Boost converter starts.
  2. Battery charging is enabled (CE pin is low, EN_CHG = 1)
  3. Without any thermal fault on TS
  4. No safety timer fault

  The charger is in “end of charge status” when the charging current is below EOC current threshold, battery voltage is above recharge voltage threshold, and device not in AICR, MIVR, JEITA, CYC_OCP or thermal regulation.

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When battery voltage is discharged below recharge threshold (threshold setting through VRECHG register bits), the device restarts a new charging cycle automatically. After the charge is done, toggle CE pin or CHG_EN can restart a new charging cycle.

- **Battery Charging Profile**

  The device charges the battery in five status: trickle charge, pre-charge, constant current, constant voltage and back-ground charge (optional).

**Table 6. Charging Current Setting**

| Current Parameter | Default Current Setting | CHG_STAT |
|---|---|---|
| $I_{TRICKLE_CHG}$ | 100mA | 001 |
| $I_{PRE_CHG}$ | 120mA | 010 |
| $I_{CHG_REG}$ | 2A (2s)/1A (3s, 4s) | 011 (CC Mode)/100 (CV Mode) |
| $I_{EOC_CHG}$ | 200mA | 111 |

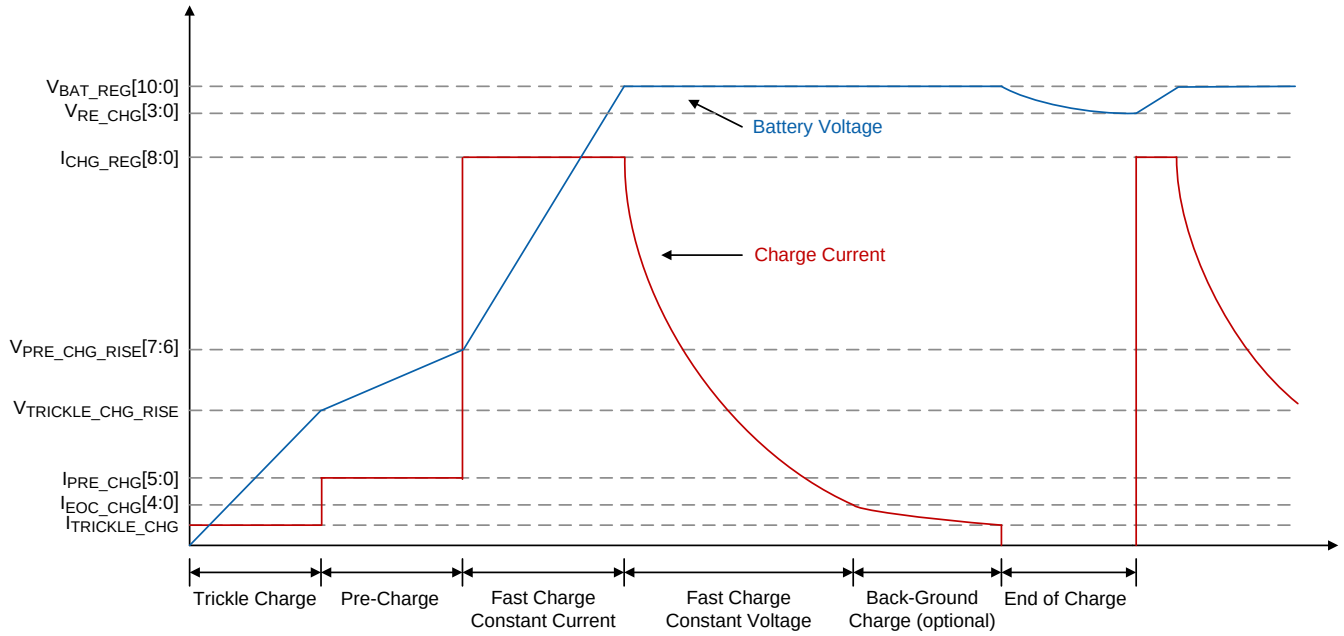


Figure 1. Charging Profile

- **End of Charge (EOC)**

  The charger enters end of charge status when battery voltage is above recharge threshold, and the charge current is below $I_{EOC_CHG}$. $I_{EOC_CHG}$ setting range is from 120mA to 1000mA with 40mA resolution. After EOC, the BATFET turns off with register EN_TE = 1 and BG_CHG_TMR = 00, and the buck boost converter keeps switching to supply power to the system. BATFET will turn on again when battery voltage is under recharge voltage threshold or device is in Battery Supply Mode during EOC.

  When EOC occurs, there are four conditions as shown in Table 7:

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Table 7. EOC Status Scenario

| | TE = 1<br>BG_CHG_TMR<br>(disable) | TE = 1<br>BG_CHG_TMR<br>(counting) | TE = 1<br>BG_CHG_TMR<br>(timeout) | TE = 0<br>BG_CHG_TMR<br>(disable) |
|---|---|---|---|---|
| **STAT Pin** | High | High | High | Low |
| **CHG_STAT** | 111 | 110 | 111 | 101 |
| **BATFET** | OFF | ON | OFF | ON |

1. If the device triggers AICR, MIVR, JEITA, CYC_OCP or thermal regulation status during charging, the actual charging current will be less than the programmed value. In this condition, EOC function will be disabled, and the safety timer's counter clock rate will be half.
2. The back-ground charge can be applied after EOC is detected. The back-ground charge is enabled by setting register BG_CHG_TMR and EN_TE = 1 only. When back-ground charge occurs, the CHG_STAT is set to 110, and the BATFET will turn off after back-ground charge timer expires.
3. The BG_CHG_TMR gets reset at one of the following conditions:
   - EN_CHG disable to enable
   - EOC status re-trigger
   - EOC_RST bit is set
   - REG_RST bit is set
   - RST_ALL bit is set

   An INT pulse is asserted to host when entering back-ground charge and back-ground charge timer expires.
4. When DIS_EOC_FCCM = 1, the IEOC accuracy will lower than Electrical Characteristic table. The device use DIS_EOC_FCCM = 0 to increase accuracy, please refer to MIVR function for application notice.

- **Optimized VDS on BATFET**

  The device deploys power path function with BATFET separating system from battery. The minimum system voltage is set by register VSYSMIN. The default VSYSMIN setting is controlled by PROG pin.

  When the battery voltage is under VSYSMIN setting, the BATFET operates in saturation mode as LDO and the system voltage is typically 200mV above the VSYSMIN setting. When the battery voltage rises above VSYSMIN, BATFET turns fully on to minimize $R_{DS(ON)}$ for optimizing VDS (voltage different between VSYS and VBAT) on BATFET.

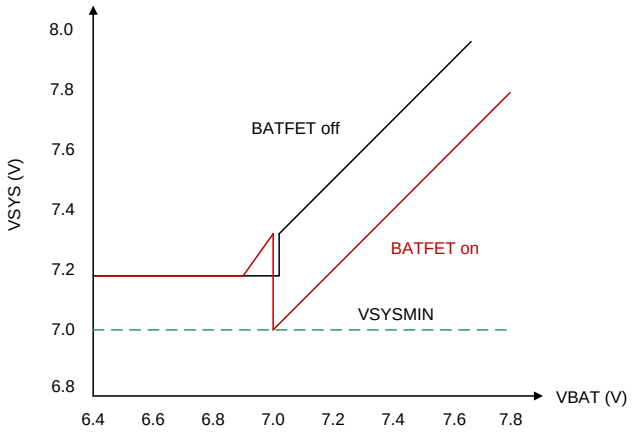


Figure 2. VSYS vs. VBAT for 2s Battery

When BATFET turns off and battery voltage is above VSYSMIN, the system is regulated at typically 300mV above battery voltage. The status register VSYSMIN_STAT = 1 when the system is in minimum system voltage regulation.

- **DIS_LDO Mode**

  When the battery voltage is under VSYSMIN setting, the BATFET operates in saturation mode as LDO, and the maximum charge current will be limited under 2A. The device supports disabling LDO mode via register DIS_LDO set to 1 by the host. When DIS_LDO = 1, the BATFET turns fully on even when battery voltage is under VSYSMIN setting, and the VSYS will not regulate on VSYSMIN setting. In DIS_LDO mode, the charge current follows the

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ICHG_CTRL/IPRE_CHG setting. The DIS_LDO mode only operates when battery voltage is above $V_{TIRCKLE_CHG_RISE}$.

### Power Management System

To apply maximum current and avoid over loading from the power source on VBUS, the device's Power Management System continuously monitors the power source voltage and current. When power source is overloaded, either the current exceeds the AICR or the voltage drops to MIVR, the device will reduce the charge current to priority power energy for system.

When the charge current is reduced to zero, but power source still triggers AICR or MIVR, the VSYS starts to drop. Once the VSYS drops under VBAT, the device automatically changes to battery supply mode, and the BATFET turns fully on and battery starts to discharge so that the system is supported from both battery and power source.

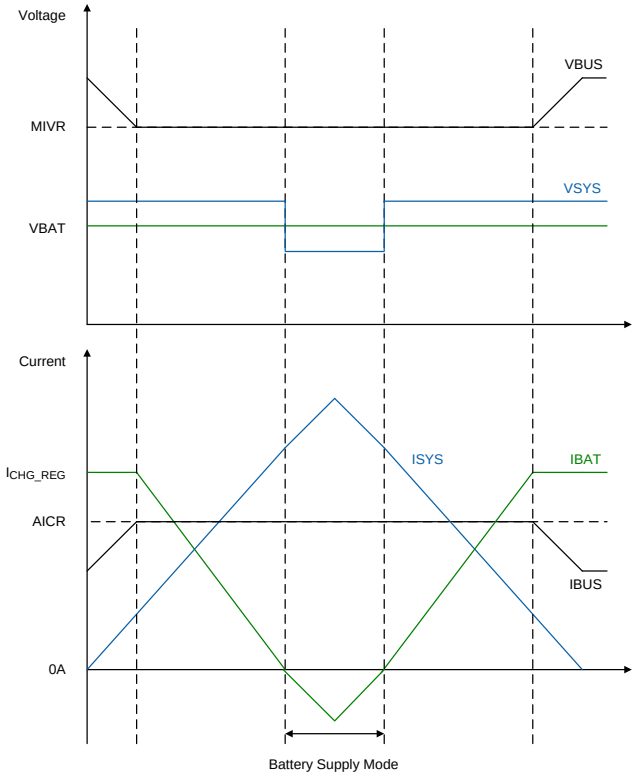


Figure 3. Power Management System

- **Battery Supply Mode**

  During charge status, when voltage difference between VBAT and VSYS is above 50mV, the BATFET turns on and the BATFET gate regulates the gate driver of BATFET to minimize VBAT-VSYS voltage to stay at 25mV to prevent entering and exiting the battery supply mode frequently. When the voltage of VBAT-VSYS is below 0mV, the charger exits the battery supply mode, and starts to charge battery.

- **JEITA Protection During Charge Mode**

  The device provides a single thermistor input for temperature monitor.

  To achieve battery thermal protection, JEITA guidelines were released in 2007.

  To start a charge cycle, the voltage on TS pin must be in the T1 to T4 range. The device will stop charging if the battery temperature is lower than T1 (Cold) or higher than T4 (Hot).

  In this case, the JEITA_COLD_STAT = 1 or JEITA_HOT_STAT = 1 and an INT is asserted to the host.

  In cool temperature range (T1 to T2), the charge current is reduced to 50% or 25% of $I_{CHG_REG}$ (configured by JEITA_ISET_COOL).

  In warm temperature range (T3 to T4), the voltage setting of $V_{BAT_REG}$ is reduced or the same as $V_{BAT_REG}$ (configured by JEITA_VSET_WARM).

  The device provides more flexible settings than JEITA requirement.

  In cool temperature range (T1 to T2), the charger can set voltage of $V_{BAT_REG}$ (configured by JEITA_VSET_COOL).

  In warm temperature range (T3 to T4), the charge current can be reduced to 50% or 25% of $I_{CHG_REG}$ (configured by JEITA_ISET_WARM).

  The device supports temperature threshold setting for COOL (T2) and WARM (T3) by register TS_COOL and TS_WARM.

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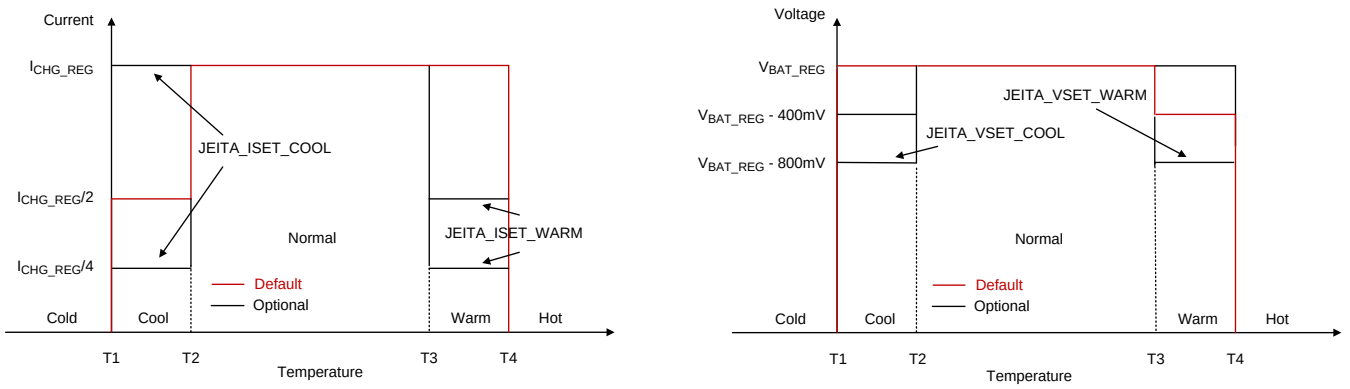


Figure 4. JEITA Protection for Charging Current and Voltage

There are four sections implemented for JEITA protection. Based on $R_{HOT}$ and $R_{COLD}$, $R_{TS1}$ and $R_{TS2}$ can be calculated with equation (1) and (2). Herein, $R_{HOT}$ is the NTC resistance of battery over-temperature threshold, and $R_{COLD}$ is the NTC resistance of battery under-temperature threshold.

$$R_{TS1} = V_{REGN} \times [(1/V_{T1} - 1/V_{T4}) / (1/R_{COLD} - 1/R_{HOT})] \quad \text{.....(1)}$$

$$R_{TS2} = R_{TS1} \times [1/(V_{REGN} / V_{T1} - R_{TS1} / R_{COLD} - 1)] \quad \text{.....(2)}$$

- **Thermal Protection During OTG Mode**

  To start a OTG mode to discharge from battery, the voltage on TS pin must be in T0 to T4 range. The device will stop converter if the battery temperature is lower than T0 (OTG_COLD) or higher than T4 (OTG_HOT). In this case, the JEITA_COLD_STAT = 1 or JEITA_HOT_STAT = 1 and an INT is asserted to the host.

  Once temperature returns to normal range, the OTG mode is recovered.

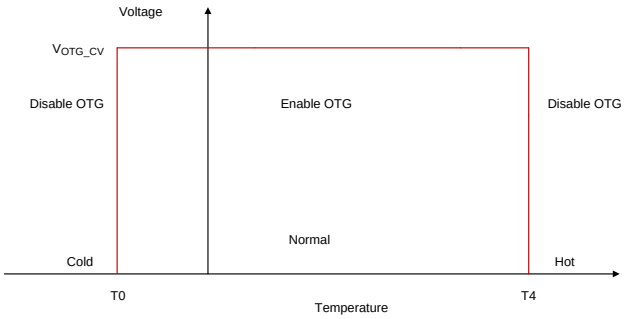


Figure 5. Thermal Protect during OTG Mode

The device supports temperature threshold setting for COLD (T0) and HOT (T4) by register OTG_COLD and OTG_HOT.

### Charging Safety Timer

The device has safety timer to prevent abnormal charging time due to poor battery condition. The device can be set EN_TRICHG_TMR, EN_PRECHG_TMR and EN_FASTCHG_TMR for each charging stage. When the safety timer expires, the device stops charging, the TRICHG_TMR_STAT, PRECHG_TMR_STAT, or FASTCHG_TMR_STAT = 1, and an INT is asserted to the host. The safety timer can be disabled by the host.

**Table 8. Charging Safety Timer**

| VBAT | Safety Timer |
|---|---|
| < $V_{TRICKLE_CHG}$ | 1 hour |
| < $V_{PRE_CHG}$ | 0.5 hours, 2 hours (Default) |
| > $V_{PRE_CHG}$ | 5 hours, 8 hours,<br>12 hours (Default), 24 hours |

When the charger in AICR, MIVR, JEITA cool, JEITA warm, thermal regulation or CYC_OCP, the safety timer's counter clock rate will be half.

For example, if charger in AICR status, and timer setting is 12 hours, the actual safety timer will expire in 24 hours. The extended charge timer setting can be disabled by setting TMR2X_EN = 0.

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The safety timer will be reset by:

1. Toggle $\overline{CE}$ pin
2. CHG_EN disable/enable
3. Safety timer disable/enable
4. REG_RST or RST_ALL is set.
5. System Power Reset

### Adaptive Input Current Control

The AICC function provides an adaptive AICR setting to prevent input voltage drops. When the input power source is overcurrent and the VBUS drops to the MIVR level, set EN_AICC bit to 1, the device will automatically decrease AICR level step by step until exit MIVR event. Once AICC is finished, EN_AICC bit keeps at 1 and the adaptive AICR setting is updated to register IAICC, AICC_STAT = 10 and an INT is asserted to the host to indicate AICC_FLAG.

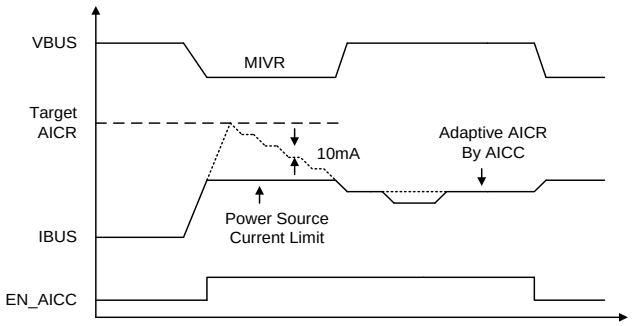


Figure 6. AICC Enable

The device supports re-enable AICC function by setting FORCE_AICC = 1, after AICC done, the FORCE_AICC goes back to 0. FORCE_AICC can be set to 1 after EN_AICC enable. The AICC function only is enabled when EN_AICC = 1.

### MediaTek Pump Express+ (MTK, PE+)

The device can provide an input current pulse to communicate with an MTK-PE+ high voltage adapter. When PE_EN bit is enabled, the device can increase or decrease adapter output voltage by setting PE10_INC or PE20_CODE to the desired value. After enabling PE function, the device will generate a VBUS current pattern for the MTK-PE+ adapter to automatically identify whether to increase or decrease output voltage.

Once the PE pattern is finished, PE_EN bit will clear to 0, and an INT is asserted to the host to indicate PE_DONE_FLAG.

### Watchdog Timer (WDT)

When the device is controlled by host, most of the registers can be programmed by host. The host has to write WD_RST = 1 to reset counter before watchdog timeout and it can disable WDT function by setting WATCHDOG bits to 00, SDRV_CTRL bits to 01 or 10.

When the watchdog timer expires, WDT_STAT and WDT_FLAG turn to high, $\overline{INT}$ pin is pulsed for interrupting the host, and the related registers are reset to default values. (Refer to Register Description for details). If the device is in watchdog timeout status, host can write any registers or WD _RST = 1 to return counting.

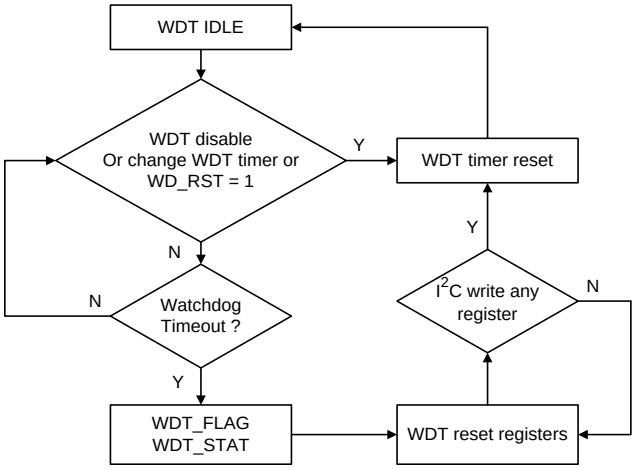


Figure 7. WDT Flow Chart

### Status Outputs and OTG Pin Control

- **Charging Status Indicator (STAT/OTG Pin)**

  The device supports multi-function on STAT/OTG pin. When register DIS_STAT = 0, the STAT/OTG pin configure as a STAT pin.

  The device indicates CHG_STAT and any charge fault on STAT pin. The STAT pin is an open drain that can be used to drive LED. The STAT pin function can be disable by setting the DIS_STAT = 1.

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Table 9. STAT Pin State

| CHG_STAT | STAT Indicator |
|---|---|
| Trickle, Pre, Fast charge, IEOC (EOC and TE = 0) | Low |
| Charge done, Back-Ground charge | High |
| Not charging (Without any charge fault) | High |
| Not charging (VBAT_OVP/VSYS_OVP/VBUS_OVP/OTP/Safety timer timeout) | Blinking at 1Hz |

- **Interrupt to Host ($\overline{\text{INT}}$ pin)**

  The device reports IRQ to host by the $\overline{\text{INT}}$ pin, which is an open drain output.

  The $\overline{\text{INT}}$ pin generates a pulse low with 256μs when IRQ event occurs.

  When an IRQ occurs, the device pulses an $\overline{\text{INT}}$ to the host and keeps IRQ event in register 0x28 to 0x2D and 0x4D until the host reads the IRQ registers. Before the host reads IRQ registers to clean IRQ events, the device will not send any $\overline{\text{INT}}$ pulse again unless any new event occurs.

  The IRQ events in register 0x28 to 0x2D are unmasked by default, and in register 0x4D is masked by default.

### Fast Role Swap (FRS)

The device supports multi-function on STAT/OTG pin. When register DIS_STAT = 1 and OTG_PIN_EN = 1, the STAT/OTG pin is configured as an OTG pin.

The device supports Fast Role Swap (FRS) by the following registers setting and steps:

1. Set DIS_STAT = 1 and OTG_PIN_EN = 1
2. The device starts charging, the CHG_STAT is not in the Not charging status.
3. Set EN_OTG = 1 and OTG_EN_CONTROL = 1

When adapter plugs out, after VBUS drops lower than VMIVR setting, and OTG pin is pulled up to high, the device translates from charge mode to OTG mode. Refer to OTG Mode Operation for detailed OTG setting.

### Seamless

The device supports Seamless to automatically translate device from charge mode to OTG mode to keep VBUS voltage output after adapter plugs out.

The device starts Seamless by the following registers setting and steps:

1. The device starts charging, the CHG_STAT is not in the Not charging status
2. Set SEAMLESS_CONTROL not at 00

When adapter plugs out, after VBUS drops lower than VMIVR setting, the device automatically translates from charge mode to OTG mode to keep VBUS voltage on

VOTG setting. The register EN_OTG auto set to 1 and SEAMLESS_CONTROL set to 00 by device. Refer to OTG Mode Operation for detailed OTG setting.

### ADC Conversion Operation

The device supports 16-bit resolution and 11 channels ADC for device information monitoring. The ADC operation is set when ADC_EN = 1, and set ADC_CONV_CTRL for One shot mode or Continuous mode.

After power-on reset (POR), when ADC_EN = 1, the ADC results are updated to the register for each channel after ADC conversion. In One-shot mode, an INT pulse is asserted to the host to indicate ADC_DONE.

The IBAT_ADC and IBUS_ADC support charging current sensing in charge mode, and discharging current sensing in OTG mode, which report with 2's complement for ADC result. With only battery, the device only provides IBAT_ADC for discharging current sensing, in this case, the register IBAT_PIN_EN also must be set to 1, and the IBAT_ADC will report 2's complement result for ADC result.

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When TS_ADC, DP_ADC and DM_ADC is enabled, the register EN_HZ must be set to 0. During ADC conversion, the REGN turns on even if the device is only with battery, and RENG keeps on when ADC operates in Continuous mode.

### DP/DM Output Control Manual Mode

The device supports DP/DM output control manual mode by programmed DP_CTRL/DM_CTRL. When DP_CTRL/DM_CTRL is not set at 000, the EN_HZ also must be set to 0, after REGN turns on, the manual control output voltage will be provided on DP/DM.

When adapter plugs in, the device will ignore manual control setting during BC1.2 detection. When BC1.2 is done, an INT is asserted to the host to indicate BC1.2_DONE and DPDM_DONE, and then the manual control will be enabled.

### DP/DM HOST Mode

The device supports HOST mode to configure the DP/DM as a SDP/CDP/DCP port compatible to standard BC1.2 by programmed HOST_MODE.

### Protections

- **VBUS Overvoltage Protection in Charge Mode**

  If VBUS voltage is over $V_{BUS_OVP}$ rising threshold, the device stops switching immediately and an INT pulse is asserted to the host. When VBUS overvoltage, the status VBUS_OVP_STAT = 1 and the CHG_STAT = 000 for stop charging. The device resumes to normal operation when VBUS voltage drops below the $V_{BUS_OVP}$ falling threshold.

- **VBUS Overvoltage Protection in OTG Mode**

  If VBUS voltage is over $V_{OTG_OVP}$ rising threshold, the device stops switching immediately and an INT pulse is asserted to the host. When VBUS is overvoltage, the status OTG_OVP_STAT = 1. The device resumes to normal operation when VBUS voltage drops below the $V_{OTG_OVP}$ falling threshold.

- **VAC Overvoltage Protection**

  If VAC voltage is over $V_{AC_OVP}$ setting (programmable by VAC_OVP bits), the device sets EN_ACDRV = 0 to turn off external ACRBFET, and an INT pulse is asserted to the host. For example, if VAC1 voltage over $V_{AC_OVP}$ setting, the EN_ACDRV1 is set to 0, the status VAC1_OVP_STAT = 1. The device resumes to normal operation when VAC1 voltage drops below the $V_{AC_OVP}$ falling threshold.

- **IBUS Overcurrent Protection in Charge Mode**

  The device monitors currents between VBUS and PMID to provide overload protection. If the IBUS current is over $I_{BUS_OCP}$ threshold, the device will set EN_HZ = 1 to stop switching immediately, also set DIS_ACDRV_EN = 1 to turn off external ACRBFETs and an INT pulse is asserted to the host. The IBUS overload protection can be disabled by setting EN_IBUS_OCP to 0.

- **OTG Undervoltage Protection**

  The device monitors OTG output voltage and current to provide VBUS short circuit protection. If VBUS voltage is under $V_{OTG_UVP}$ threshold, the device stops switching. If short circuit is detected on VBUS, the OTG will hiccup 7 times. If converter retries are not successful, EN_OTG bit will set to 0 to disable OTG mode an INT pulse is asserted to the host to indicate OTG_UVP. The hiccup can be disabled by DIS_VOTG_UVP_HICCUP to 1; when hiccup is disabled, the converter continues switching even if VBUS voltage is under $V_{OTG_UVP}$ threshold.

- **VSYS Overvoltage Protection**

  If VSYS voltage is over $V_{SYS_OVP}$ rising threshold, the device stops switching immediately and an INT pulse is asserted to the host. When VSYS is overvoltage, the status VSYS_OVP_STAT = 1. The device provides resistance sink source on VSYS to bring down the VSYS voltage. The device resumes to normal operation when VSYS voltage drops below the $V_{SYS_OVP}$ falling threshold.

- **VSYS Undervoltage Protection**

  The device monitors VSYS output voltage to provide VSYS undervoltage protection. If VSYS voltage is under $V_{SYS_UVP}$ threshold, the device stops switching and an INT pulse is asserted to the host. If short circuit is detected on VSYS, the converter will hiccup 7 times. If converter retries are not successful, EN_HZ bit will be setting to 1 to enter HZ mode. Re-plug in adapter or set EN_HZ to 0 can exit HZ mode

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and the converter restarts to switch. The hiccup can be disabled by DIS_VSYS_UVP_HICCUP to 1; when hiccup is disabled, the converter continues switching even if VSYS voltage is under $V_{SYS_UVP}$ threshold.

- **VSYS Short Protection**

  The device monitors VSYS output voltage to provide VSYS short circuit protection. The VSYS short protection can only enabled by the following setting:

  1. The device must have SHIPFET
  2. The register SHIP_FET_PRESENT must be set to 1

  When short circuit is detected on VSYS, the device will set SDRV_CTRL to 10 to immediately enter Ship Mode to turn off SHIPFET and an INT pulse is asserted to the host to indicate VSYS_SHORT.

- **VBAT Overvoltage Protection**

  If VBAT voltage is over $V_{BAT_OVP}$ rising threshold, the device stops switching immediately and an INT pulse is asserted to the host. When VBAT is overvoltage, the status VBAT_OVP_STAT = 1. The device provides resistance sink source on VBAT to bring down the VBAT voltage. The device resumes to normal operation when VBAT voltage drops below the $V_{BAT_OVP}$ falling threshold.

- **IBAT Overcurrent Protection**

  The system overload protection can only be enables by the following setting:

  1. The device must have SHIPFET
  2. The register SHIP_FET_PRESENT must be set to 1
  3. The register EN_BATOC must be set to 1

  When the system is overloaded ($I_{BAT} > I_{OCP_BATFET}$), the device will set SDRV_CTRL to 10 to immediately enter Ship Mode to turn off SHIPFET and an INT pulse is asserted to the host to indicate IBAT_OCP.

- **Thermal Protection in Charge Mode**

  The device monitors the internal junction temperature to avoid overheat. When in charge mode, the thermal regulation threshold is set at 120°C (programmable by register THREG bits). When junction temperature exceeds thermal regulation threshold, the device decreases the input current limit. During thermal regulation, EOC function is disabled, the safety timer's counter clock rate will be half and an INT is asserted to the host indicate THREG.

  The thermal regulation protection actives when EN_AICR = 1.

  In addition, the device has thermal shutdown protection, the thermal shutdown threshold is set at 150°C (programmable by register TOTP bits). When the IC junction temperature exceeds thermal shutdown threshold, the converter turns off immediately and an INT is asserted to the host indicate TOTP fault. The converter is recovered when the junction temperature is below $T_{OTP}$ - $T_{OTP_HYS}$.

- **Thermal Protection in OTG Mode**

  The device monitors the internal junction temperature to avoid overheat. When in OTG mode, the thermal regulation threshold is set at 120°C (programmable by register THREG bits). When junction temperature exceeds thermal regulation threshold, the device decreases the output current limit, and an INT is asserted to the host to indicate THREG.

  The thermal regulation protection actives when IBAT_REG does not set at disable.

  In addition, the device also has thermal shutdown protection in OTG mode.

- **Poor Source Detect Protection**

  The device supports source sink on VBUS to detect whether the adapter is poor source or not. When poor source is detected, the device will hiccup 8 times. If device retries are not successful, the device will set EN_HZ = 1 and an $\overline{INT}$ is asserted to the host to indicate BAD_ADAPTER.

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**Table 10. Protection Summary**

| Channel | Threshold (Typ.) | Deglitch (Typ.) | Protection | Reset and Threshold (Typ.) |
|---|---|---|---|---|
| VBUS_OVP | $V_{BUS_OVP}$ rising | NA | Converter stop switching | $V_{BUS_OVP}$ falling |
| VAC_OVP | $V_{AC_OVP}$ rising | NA | Disable ACDRV1 or ACDRV2 to turn off external MOSFET | $V_{AC_OVP}$ falling |
| IBUS_OCP | $I_{BUS_OCP}$ rising | 2ms | REG0x0F[2] = 1 to enter HZ to stop converter switching, and disable ACDRV1 or ACDRV2 to turn off external MOSFET. | NA |
| OTG_OVP | $V_{OTG_OVP}$ rising | NA | Converter stop switching | $V_{OTG_OVP}$ falling |
| OTG_UVP | $V_{OTG_UVP}$ falling | 10ms | Converter start hiccup, after hiccup 7 times, REG0x12[6] = 0 to disable OTG. Hiccup can be programmed in REG0x13[2]. | $V_{OTG_UVP}$ rising |
| SYS_OVP | $V_{SYS_OVP}$ rising | 128µs | Converter stop switching | $V_{SYS_OVP}$ falling |
| SYS_UVP | $V_{SYS_SHORT}$ falling | 64µs | Converter start hiccup, after hiccup 7 times, REG0x0F[2] = 1 to enter HZ to stop converter switching. Hiccup can be programmed in REG0x13[3]. | $V_{SYS_SHORT}$ rising |
| SYS_SHORT | $V_{BAT}$ - $V_{SYS}$ rising to 200mV | 128µs | With external SHIPFET, when trigger SYS_SHORT, the SDRV_CTRL enter Ship mode. The SYS_SHORT protect must set REG0x14[7] to 1. | NA |
| VBAT_OVP | $V_{BAT_OVP}$ rising | 2ms | Converter stop switching | $V_{BAT_OVP}$ falling |
| IBAT_OCP | $I_{OCP_BATFET}$ rising | 3ms | With external SHIPFET, when trigger IBAT_OCP, the SDRV_CTRL enter Ship mode. The IBAT_OCP protect must have to set REG0x14[7] to 1. | NA |
| Thermal Regulation | $T_{J_THREG}$ rising | 32ms | Limit converter output power | $T_{J_THREG}$ falling |
| Poor Source Detect | $V_{BUS_MIN}$ falling | 30ms | When poor source is detected, after 8 times hiccup, REG0x0F[2] = 1 to enter HZ. | $V_{BUS_MIN}$ rising |

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### Communication Interface

The device uses I²C compatible interface by 2-wire line (SCL and SDA) to communicate with the host. The SCL and SDA pins are open drain, which needs to connect to supply voltage by pull-up resistors. The device operates as an I²C slave device with 7-bits address 53H, supports up to 3.4MHz conditionally. To start an I²C communication, beginning with START (S) condition, and then the host sends slave address. This address is 7-bit long followed by an eighth bit which is a data direction bit (R/W). The second bytes is register address. The third byte contains data to the selected register. End with STOP (P) condition.

- **I²C Time-Out Reset**

  To avoid I²C hang-ups, a timer runs during I²C activity. If the SDA keeps low longer than 1 second, the device will reset I²C to release SDA to go back to High. The I²C hang-ups reset function can be disabled by register DIS_I2C_TO = 1.

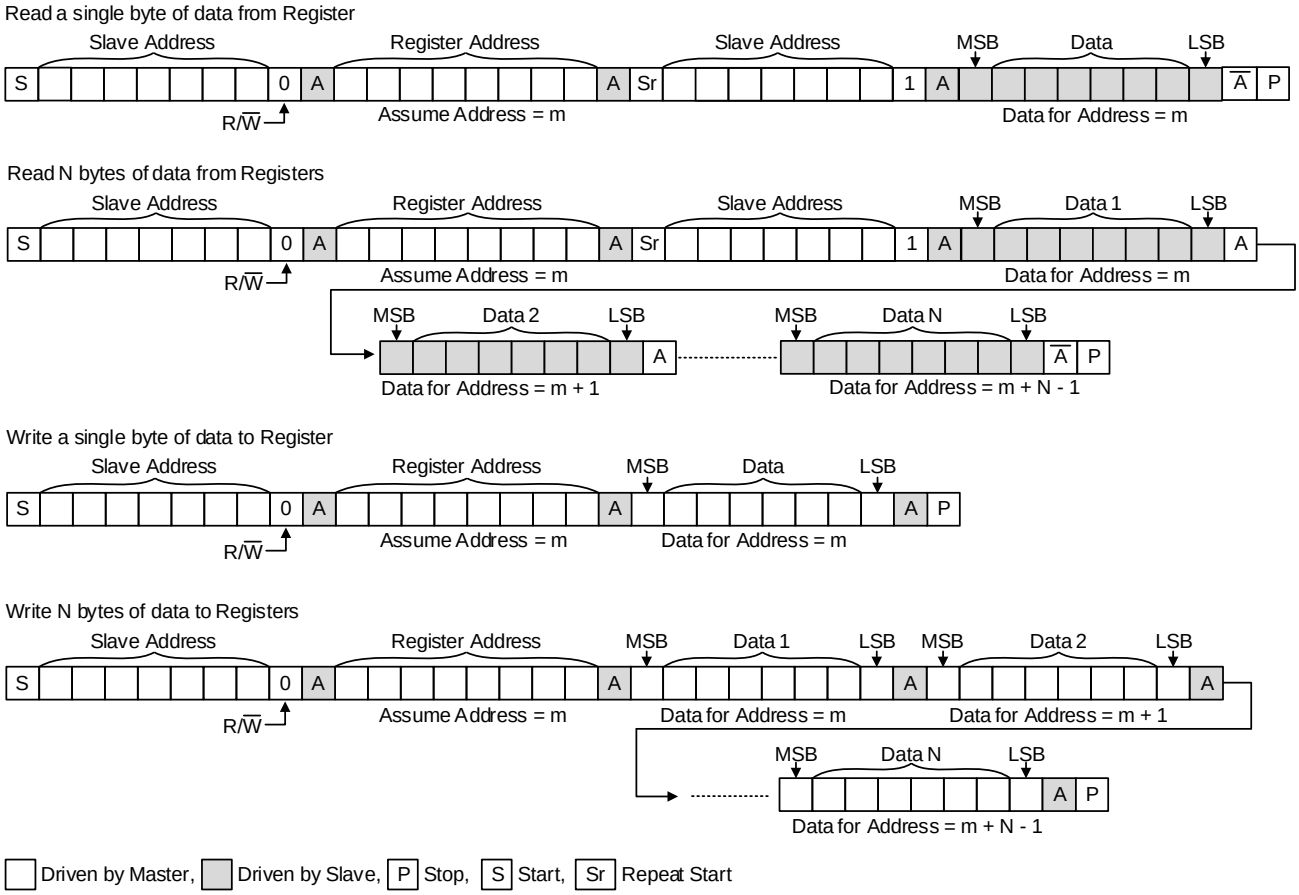


Figure 8. Read and Write Function

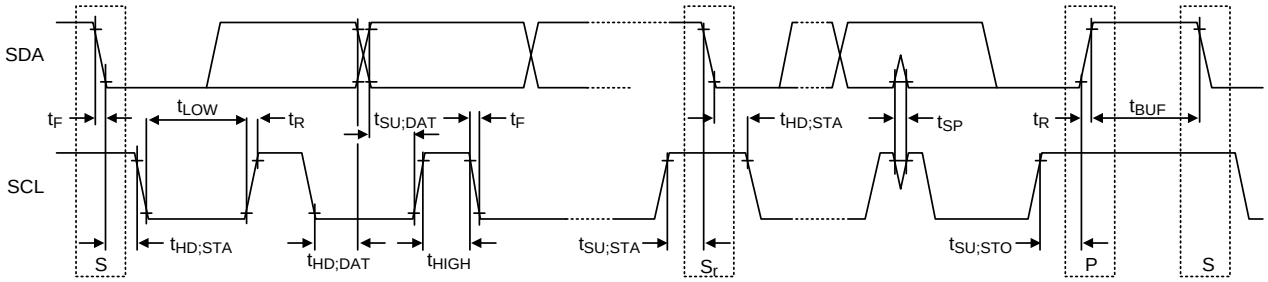


Figure 9. I²C Waveform Information

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### Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 130°C. The junction-to-ambient thermal resistance, $\theta_{JA}$, is highly package dependent. For a VQFN-29TL 4x4 (FC) package, the thermal resistance, $\theta_{JA}$, is 44°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A$ = 25°C can be calculated as below:

$P_{D(MAX)}$ = (130°C - 25°C) / (44°C/W) = 2.38W for a VQFN-29TL 4x4 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA}$. The derating curve in Figure 10 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

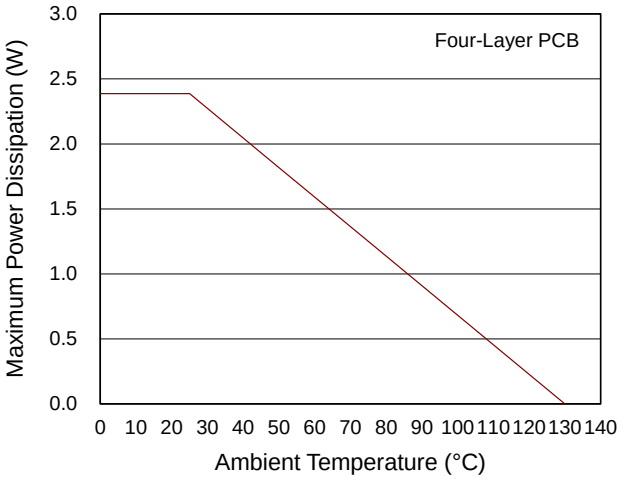


Figure 10. Derating Curve of Maximum Power Dissipation

### Layout Considerations

The RT9492 layout guidelines are shown as below, and there are several suggestions provided.

- The capacitors connected to PMID pin needs to be placed as close as possible to the IC.
- The inductor connected to SW pin needs to not only router the trace as short as possible to reduce the EMI but also make sure copper area of the trace is wide enough for the operating current.
- The capacitors connected to VSYS pin needs to be placed as close as possible to the IC. Three 10μF capacitors on Top, and two capacitors on Bottom.
- The capacitors connected to VBAT pin needs to be placed as close as possible to the IC.
- The 0.1μF Capacitor, connected to VAC1/VAC2, PMID and VSYS must be placed close to the IC.
- The GND needs to connect on TOP layer with PMID and SYS capacitors, use ground vias to connect to main ground as close as possible to the IC.

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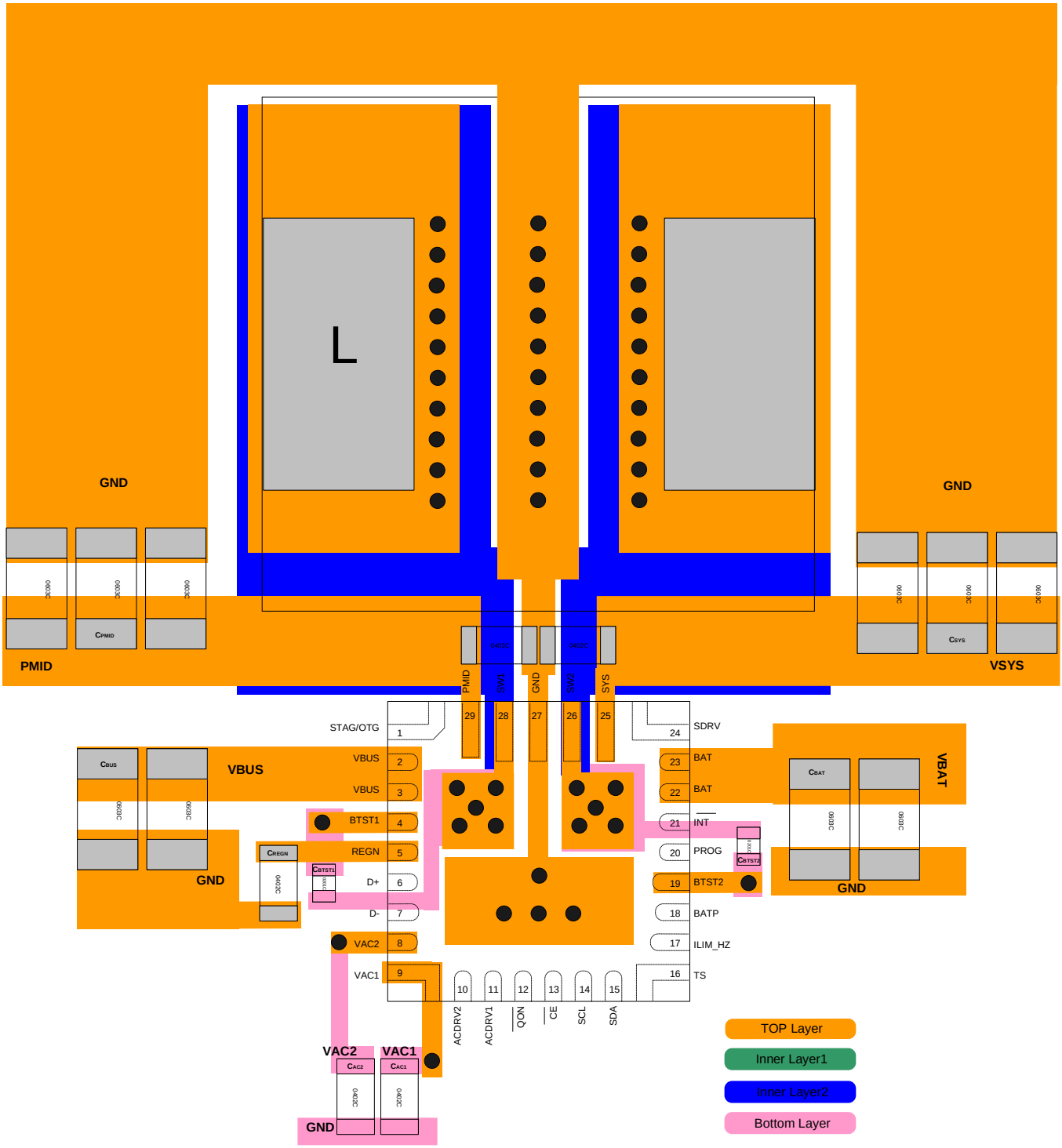


Figure 11. PCB Layout Guide

**Note 9**. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

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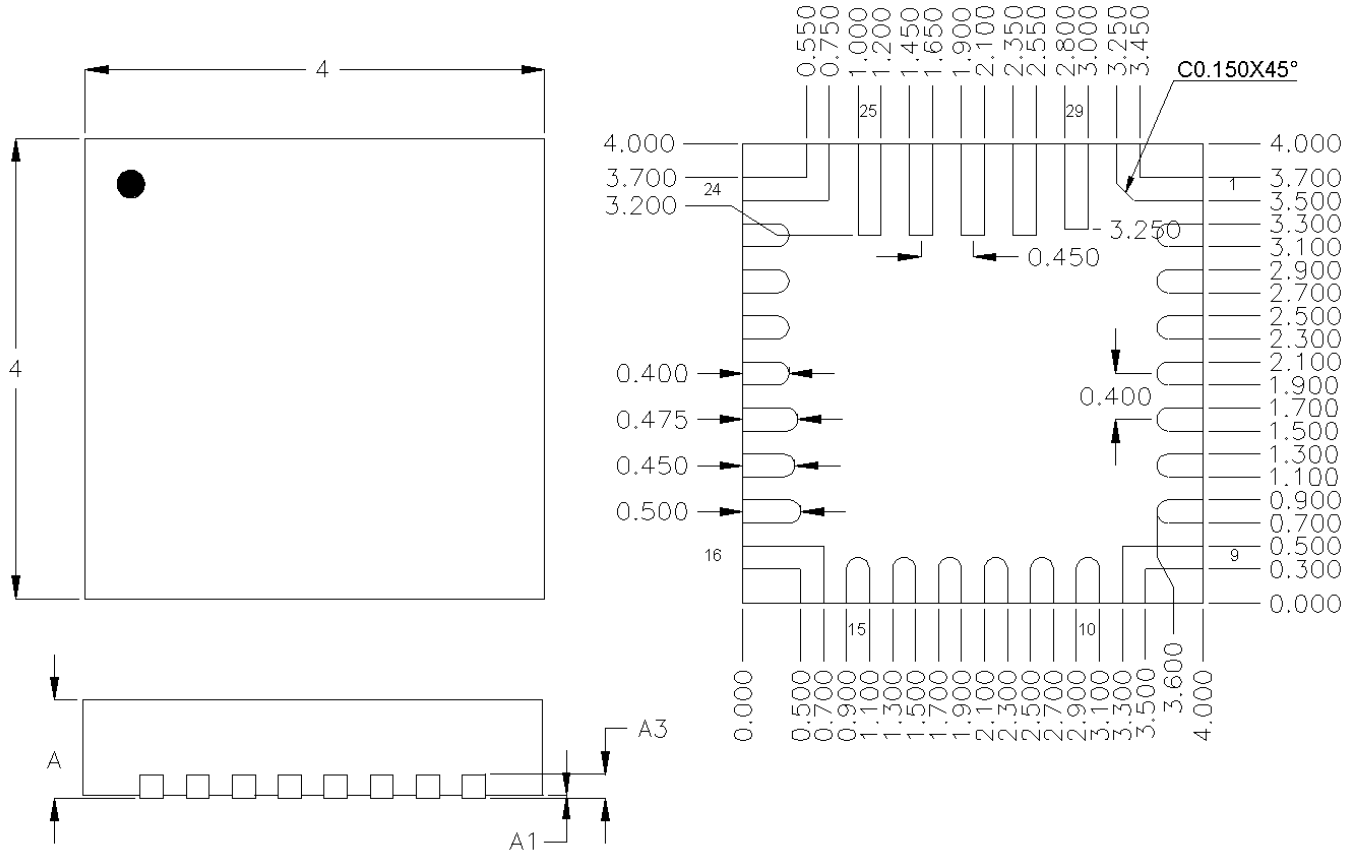
## Outline Dimension




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.800 | 1.000 | 0.031 | 0.039 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |

**V-Type 29TL QFN 4x4 Package (FC)**

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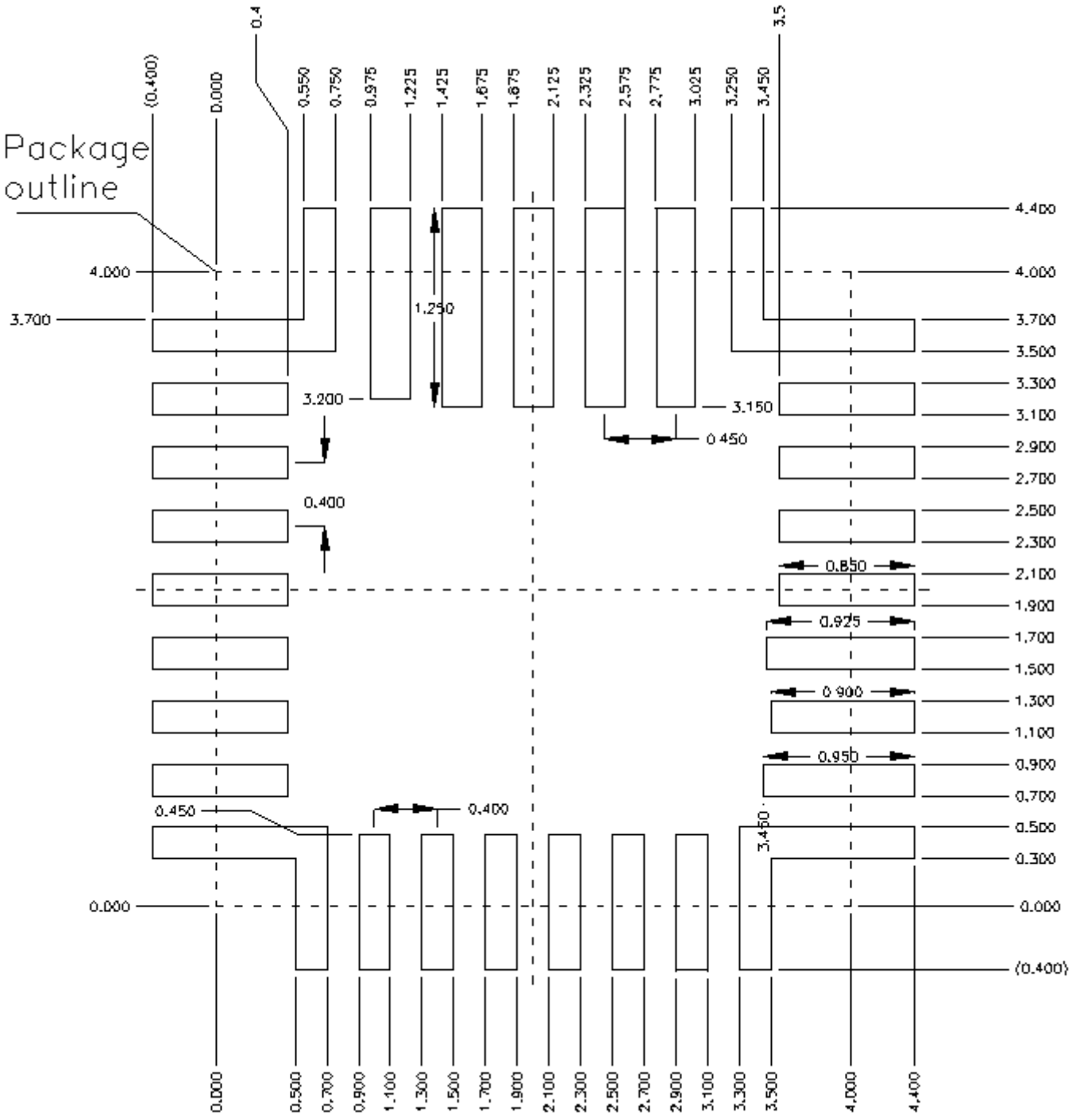
## Footprint Information




| Package | Number of Pin | Tolerance |
|---|---|---|
| V/W/U/XQFN4x4-29T(FC) | 29 | ±0.05 |

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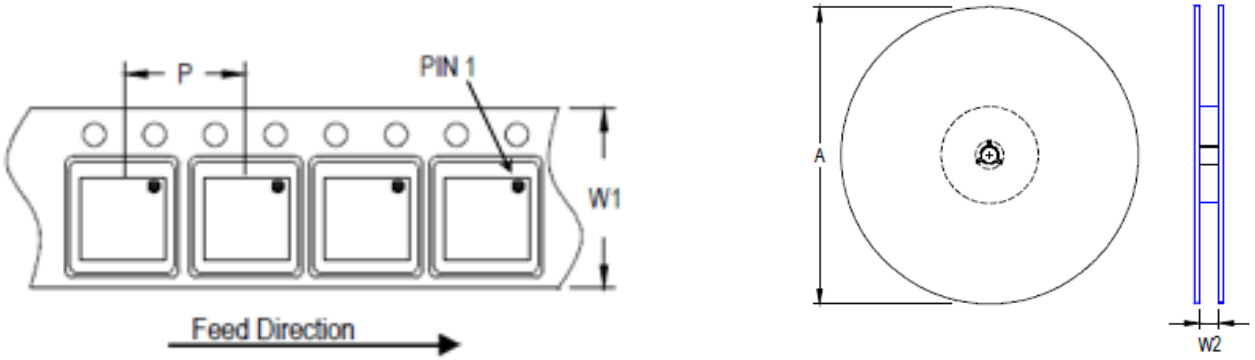
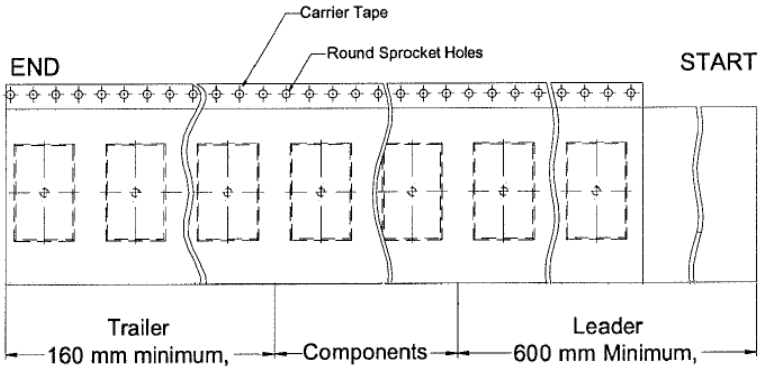
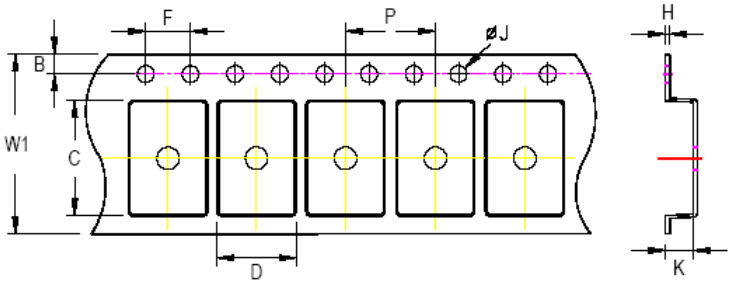
## Packing Information

### Tape and Reel Data




| Package Type | Tape Size (W1) (mm) | Pocket Pitch (P) (mm) | Reel Size (A) | | Units per Reel | Trailer (mm) | Leader (mm) | Reel Width (W2) Min./Max. (mm) |
|---|---|---|---|---|---|---|---|---|
| | | | (mm) | (in) | | | | |
| QFN/DFN 4x4 | 12 | 8 | 180 | 7 | 1,500 | 160 | 600 | 12.4/14.4 |




**C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:**

**- For 12mm carrier tape: 0.5mm max.**

| Tape Size | W1 | P | | B | | F | | ØJ | | H |
|---|---|---|---|---|---|---|---|---|---|---|
| | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Max. |
| 12mm | 12.3mm | 7.9mm | 8.1mm | 1.65mm | 1.85mm | 3.9mm | 4.1mm | 1.5mm | 1.6mm | 0.6mm |

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## Tape and Reel Packing

| Step | Photo/Description | Step | Photo/Description |
|---|---|---|---|
| 1 | Reel 7” | 4 | 3 reels per inner box **Box A** |
| 2 | HIC & Desiccant (1 Unit) inside | 5 | 12 inner boxes per outer box |
| 3 | Caution label is on backside of Al bag | 6 | Outer box **Carton A** |

| Container / Package | Reel | | Box | | | Carton | | |
|---|---|---|---|---|---|---|---|---|
| | Size | Units | Item | Reels | Units | Item | Boxes | Unit |
| QFN/DFN 4x4 | 7” | 1,500 | Box A | 3 | 4,500 | Carton A | 12 | 54,000 |
| | | | Box E | 1 | 1,500 | For Combined or Partial Reel. | | |

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**Packing Material Anti-ESD Property**

| Surface Resistance | Aluminum Bag | Reel | Cover tape | Carrier tape | Tube | Protection Band |
|---|---|---|---|---|---|---|
| $\Omega/cm^2$ | $10^4$ to $10^{11}$ | $10^4$ to $10^{11}$ | $10^4$ to $10^{11}$ | $10^4$ to $10^{11}$ | $10^4$ to $10^{11}$ | $10^4$ to $10^{11}$ |

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## Datasheet Revision History

| Version | Date | Description | Item |
|---|---|---|---|
| 00 | 2023/7/5 | Final | |
| 01 | 2023/7/20 | Modify | Ordering Information on P1 |
| 02 | 2024/5/9 | Modify | Title on P1<br>General Description on P1<br>Ordering Information on P1<br>Device Comparison on P2<br>Functional Block Diagram on P5<br>Electrical Characteristics on P8 to 19<br>Typical Application Circuit on P22, 23<br>Typical Operating Characteristics on P25, 26, 27<br>Register Description on P30, 31, 33, 39, 46, 50, 53, 55, 56, 57<br>Application Information on P63, 64, 65, 69, 70, 72, 74, 75, 76, 79, 80<br>Packing Information on P84 |

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